SILICON-GERMANIUM BICMOS AND SILICON-ON-INSULATOR CMOS ANALOG CIRCUITS FOR EXTREME ENVIRONMENT APPLICATIONS

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SILICON-GERMANIUM BICMOS AND SILICON-ON-INSULATOR CMOS ANALOG CIRCUITS FOR EXTREME ENVIRONMENT APPLICATIONS

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To my Lord and Savior, Jesus Christ.

May everything I do be worship unto You.

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SUMMARY

Extreme environments pose major obstacles for electronics in the form of extremely wide temperature ranges and hazardous radiation. The most common mitigation procedures involve extensive shielding and temperature control or complete displacement from the environment with high costs in weight, power, volume, and performance. There has been a shift away from these solutions and towards distributed, in-environment electronic systems where the critical signal processing can be closer to sensors, improving performance. However, for this methodology to be viable, the requirements of heavy radiation shielding and temperature control have to be lessened or eliminated. Consequently, silicon-germanium (SiGe) BiCMOS and scaled, silicon-on-insulator (SOI) CMOS technologies have become increasingly popular choices for extreme environment electronics. Each has their own benefits above those of basic CMOS processes, making them capable of robust operation in extreme environments. This work used those technologies to gain new understanding of the best practices in analog circuit design for both wide temperature ranges and radiation exposure.

Major accomplishments are listed below:

1. The over-temperature (−180 °C to +120 °C) and radiation (total ionizing dose and single-event latchup) validation of the SiGe Remote Electronics Unit, a first of its kind, 16 channel, sensor interface for unshielded operation in the Lunar environment [1, 2],

2. The design of two wide-temperature (−180 °C to +120 °C), total-ionizing-dose hardened, wireline transceivers for the Lunar environment [3, 4],

3. The low-frequency-noise characterization of a second-generation BiCMOS process from 300 K down to 90 K,

4. The explanation of the physical mechanisms behind the single-event transient response of cascode structures in a 45 nm, SOI, radio-frequency, CMOS technology [5],

5. The analysis of the single-event transient response of differential structures in a 32 nm, SOI, RF, CMOS technology, and

6. The prediction of scaling trends of single-event effects in SOI CMOS technologies [5].

CHAPTER I

INTRODUCTION

The label "extreme environment" can be used to cover any environment that lies outside of the commercial or military norm [6]. Often it refers to areas with wide temperature ranges, harmful radiation, high magnetic fields, corrosive materials, or any number of other disruptive elements. Examples of such environments include areas outside the Earth's protective atmosphere and the cryogenic conditions used for a variety of noise-sensitive measurements. The characteristics of extra-terrestrial environments vary extensively based on the location of exploration. Electronics operating on the Moon are required to withstand temperature swings from −230 °C in shadowing craters to +120 °C in direct sunlight. In addition, space-based electronics are exposed to many types of radiation that can cause device damage and sometimes catastrophic failure. In some cutting-edge particle experiments, thermal energy is limited to reduce noise levels and chemical interaction. Examples of temperature reduction include near the nitrogen boiling point, about 77 K [7], or even lower, approaching absolute zero [8]. For this work, extreme environments are limited to those with wide temperature ranges (−180 °C to +120 °C) and radiation exposure. Even limited to such characteristics, these environments present a multitude of challenges to electronics designers.

Continuous operation between −180 °C and +120 °C leads to drift of important device parameters such as small-signal transconductance (g_m), peak unity gain frequency (f_T), maximum oscillation frequency (f_{MAX}), threshold voltage (V_{th}), thermal voltage (V_T), and noise power spectral density (S). In designs without wide-temperature

compensation, circuit characteristics, such as gain, bandwidth, phase margin, and input offset, consequently drift. Without special design corrections, these specification shifts will cause failure of electronic systems.

Currently, the common practice is to protect electronics from extreme-environment exposure by either placement outside the environment or extensive shielding and temperature control inside the environment. In extraterrestrial applications "warm-boxes" or "electronics vaults" have provided the shielding and heating necessary to protect crucial components. Unfortunately, both of these solutions, displacement or protection, increase weight, volume, power, and complexity. For example, the electronic vault for the Juno spacecraft shown in Figure 1 weighed approximately 500 pounds [9].

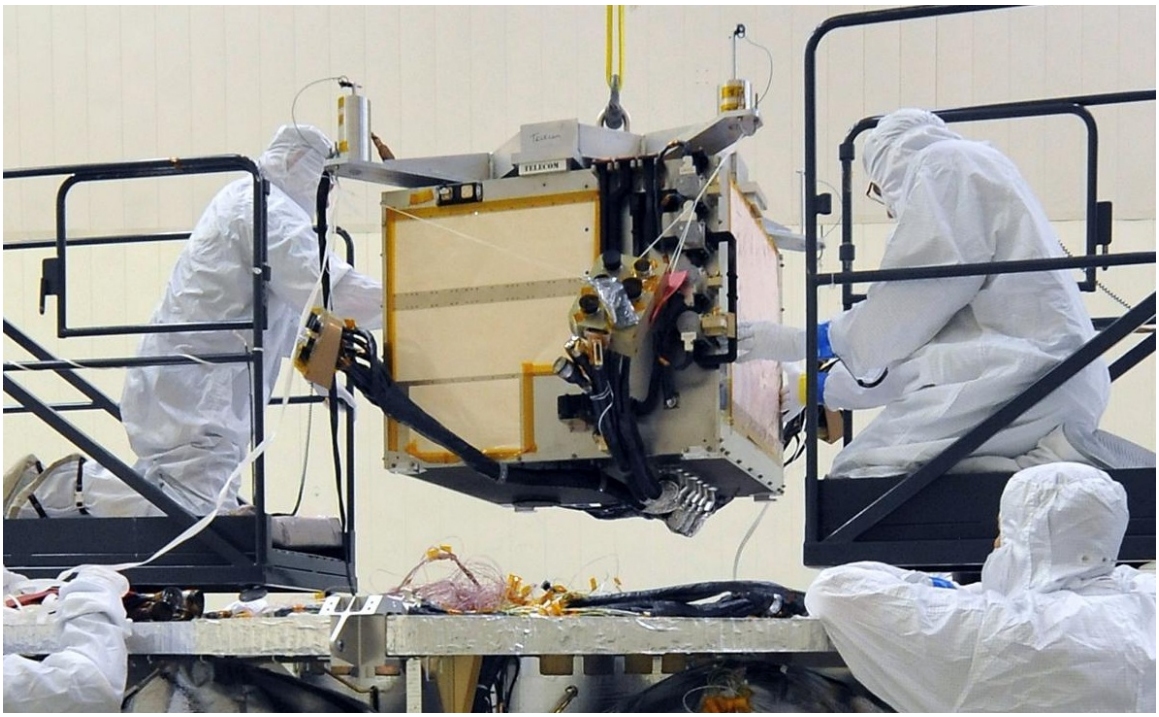


Figure 1: The radiation vault for NASAs Juno spacecraft weighed 500 pounds after [9].

There has been a recent paradigm shift that advocates moving away from centralized warm-boxes or displaced electronics and towards system-on-chip and system-in-package solutions that do not require environmental control. These distributed,

in-environment electronics have major benefits in remote sensing where the initial, critical signal processing can be adjacent to sensors rather than far away, resulting in added noise. Distributed electronics also allow for point-of-load contact, enabling better control where extensive wiring induced parasitics that limited the performance of feedback networks. However, for distributed, in-environment electronics to be a viable alternative to their centralized counterparts, the requirement of heavy radiation shielding and temperature control must be lessened or eliminated. For this to be a possibility, a technology platform is needed that meets rigorous specifications while being extreme environment tolerant.

1.1 Silicon-Germanium Technology

The earliest practical transistors were bipolar junction transistors (BJTs). These transistors rely predominately on diffusion current across PN junctions for current flow. Band diagrams showing different bias states of an evenly doped PN diode are shown in Figure 2. At zero bias, carriers naturally defuse across the junction until charge buildup on each side of the junctions creates an electric field strong enough to counteract the diffusion. When reversed biased, carriers cannot diffuse across the junction, and the electric field increases in magnitude. At forward bias the bands are shifted, and current flow occurs proportional to the carrier concentrations near the conduction and valence bands. The carrier concentrations exponentially increase near the bands, so linear bias voltage steps result in exponential current flow. If the diode is unevenly doped, the current will be proportionally made up of the types of carries present in the more highly doped region.

The BJT is made up of the combination of two PN junctions. The most common type of BJT is the NPN and a conceptional diagram is shown in a figure. The lowest potential node is the n-type emitter so called because it emits the electrons that act as the primary carriers in the device. The p-type central area is the base. Its

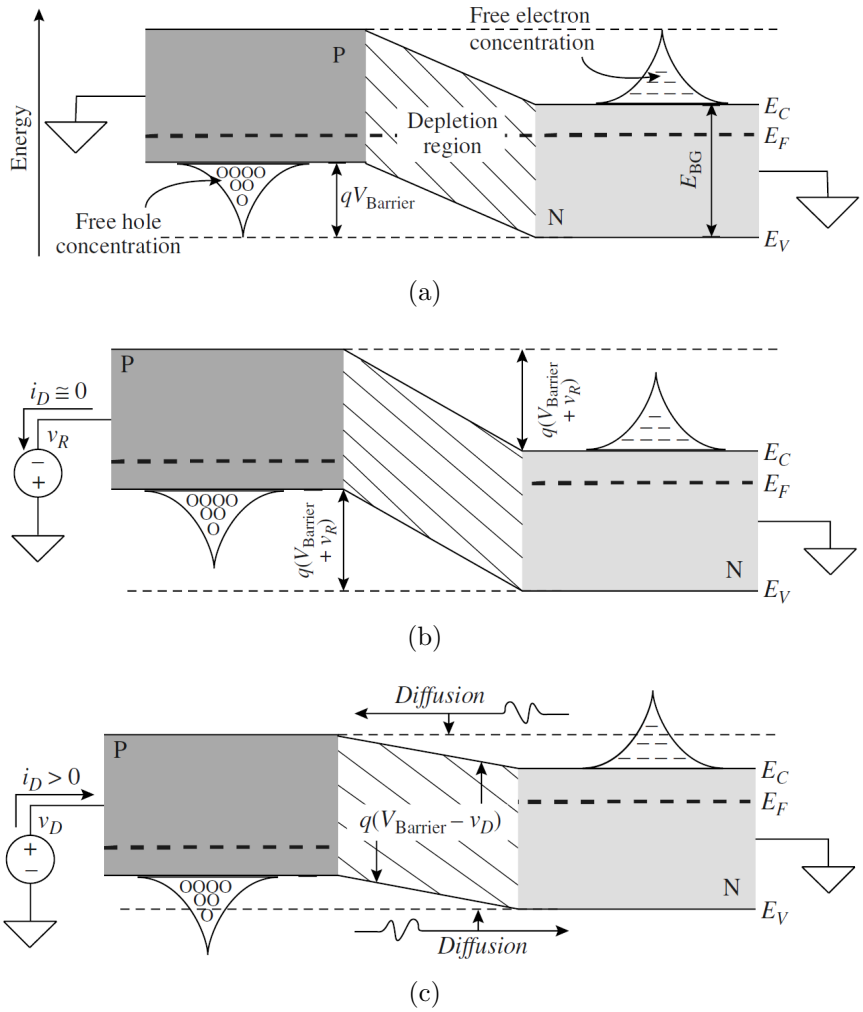


Figure 2: PN junction diode band diagrams (a) unbiased, (b) reverse biased, and (c) forward biased. (After [10])

name originates from the first transistor prototypes where the base was the physical foundation of the device. The other n-type section is the collector. It collects the electrons from the emitter.

Two of the key features of an optimized BJT are that the electron path through the base must be very short and the emitter must be much more highly doped than the base. To show why these features are important, the most desirable mode of operation, forward active, will be explained. In this mode, the base-emitter (BE) PN junction is forward biased, and the base-collector (BC) PN junction is reverse biased. Forward biasing the BE junction results in carrier diffusion across the junction including hole current from the base and electron current from the emitter. Because the emitter is much more highly doped than the base, a proportionally higher amount of electrons flow than holes. At the same time, the reverse biasing of the BC junction creates an electric field in the junction that acts to pull electrons out of the base and into the collector. Because the base is very thin, a high percentage of the electrons from the emitter travel through the base and out the collector, avoiding recombination with the holes in the p-type base. When optimized, the output collector current will be much greater than the input base current, resulting in current gain. Typical current gain figures are on the order of 100. Notice that if either the electron path in the base is long or the emitter is not more highly doped than the base, then the input current will be equal to or higher than the output current.

At the same time, not all device characteristics benefit from these two conditions. One of limiters of bipolar transistor speed is base resistance. The simplest way to reduce base resistance is to increase base doping, but higher base doping results in higher base current and lower current gain. Modern techniques to increase the speed of bipolar transistors include the use of germanium (Ge). The use of germanium as a stand-alone semiconductor has been possible for decades, but it was also theorized that the introduction of Ge into silicon could open the door for very interesting device

performance improvements by manipulating the material band gap. Due to process improvements leading up to the 1990s, the idea of the practical introduction of Ge into a Si BJT became a reality.

1.1.1 Silicon-Germanium Heterojunction Bipolar Transistors

At first glance, the silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) is very similar to a Si BJT except for the Ge content present in the base area of the device. The addition of Ge acts to locally reduce the band-gap based on the percentage content. Adding Ge in an gradient increasing from the emitter to the collector results in a matching conduction band gradient, which induces an electric field in the base, assisting electron transport across it. A band diagram of a SiGe HBT in forward active mode is shown in Figure 3. In addition to the gradient effect, the Ge content level at the BE junction helps to increase current gain. Because the band-gap shrinkage mainly affects the conduction band, the electron diffusion current is boosted while the hole current remains the same. Modern SiGe HBTs often contain a combination of flat and gradient Ge concentrations to get benefits in both electron transport and current gain.

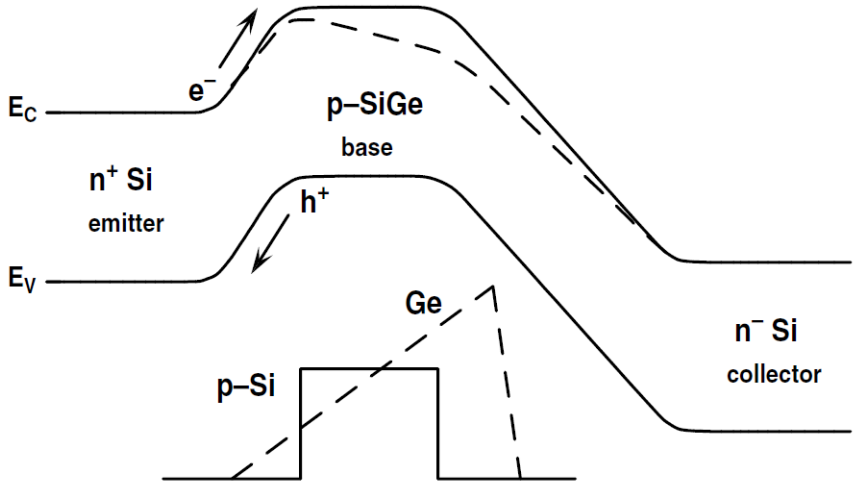


Figure 3: A band diagram of a SiGe HBT showing Ge content and the resulting band bending. (After [11])

1.2 Scaled Silicon on Insulator CMOS

With continued scaling, CMOS remains the dominant player in the electronics industry. The famous Moores Law predicting exponential increase of component count on chip has become a realization [12]. At the same time, silicon-on-insulator (SOI) technology has spurred on the growth of radio frequency (RF) silicon-on-insulator (SOI) CMOS processes due to their superior high-frequency capability. IBM researchers set a new record for high speed performance in a CMOS platform with record of peak f_T near 500 GHz with their 45 nm, partially-depleted, SOI CMOS technology [13]. Cascode structures in this technology have been shown to have appreciable power gain and cut-off frequencies above 350 GHz [14]. IBMs release of a 32-nm SOI technology may hold similar potential [15].

SOI CMOS had a number of advantages over bulk CMOS, but it also requires special design considerations. Possibly the largest design decision specific to SOI CMOS is the choice between floating-body and body-contacted devices. The implications of a floating-body MOS device include reduced reliability and variations of threshold voltage during operation as the body voltage increases above that of the source terminal. The reliability concern stems from the creation of hot carriers in the channel region [14]. When hot carries create excess electron-hole pairs in a raised-body-voltage condition, it can result in diffusion current across the source-body junction that reinforces creation of hot carriers, and in extreme cases, it can cause a runaway condition that leads to catastrophic failure. Also due to the raised body voltage, the threshold voltage can vary much the same way it is known to vary in bulk processes based on body bias.

The most common way to mitigate the reliability and threshold voltage problems with floating-body devices is the use of body contacts in SOI devices. The body contacts ensure a specific bias voltage for the device body. Unfortunately, the body contacts come with their own set of drawbacks. First, body contacts add area to the device.

In an industry that relies on the continued shrinking of devices, additional area is the worst of penalties. Area increases in single devices can be multiplied by the billions on modern processor and memory chips. Second, body contacts effectively add another junction to the device. One of the greatest strengths of SOI devices is the lack of junction isolation that is a significant source of parasitic capacitance in bulk devices. The introduction of a body contact returns some of that capacitance and, in turn, reduces the speed of the device. The application will determine which drawback is worse: size for digital chips, speed for RF.

In an effort to reduce the penalty of body contacts, a number of body-contacting schemes have been introduced. Diagrams of a few schemes are shown in Figure 4 and are named for their shape [16]. Significant work has been dedicated to studying the tradeoffs between each scheme [13, 17]. If contacting is required, the notched-T contact is preferred for high-frequency designs because of its small footprint and lower added capacitance compared to the others.

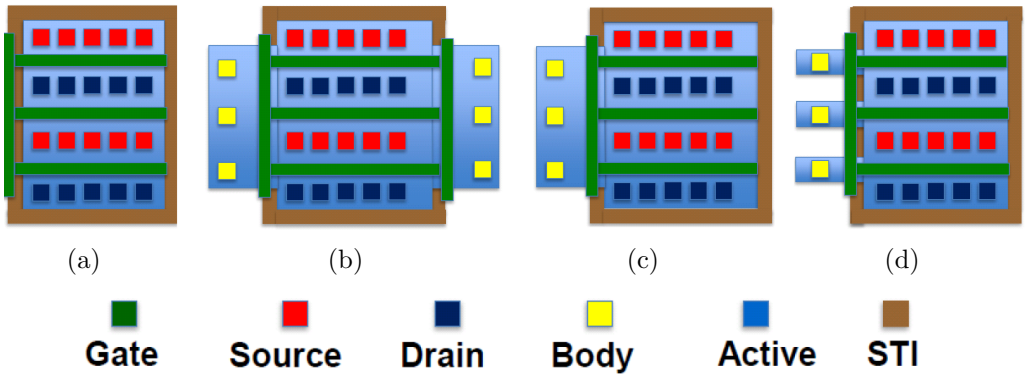


Figure 4: SOI CMOS body-contacting schemes: (a) floating body, (b) H body, (c) T body, and (d) notched-T body. (After [16])

1.3 Radiation Effects in Semiconductors

Electronics exposed to radiation suffer from three categories of harmful effects. First, total ionizing dose (TID) effects are the result of ionizing energy creating electron-hole pairs in semiconductor materials. It is most detrimental in oxides where holes

become trapped at the semiconductor-oxide interfaces, creating recombination traps. Second, displacement damage (DD) effects are derived from the actual dislocation of lattice atoms in semiconductor materials. Last, single-event effects (SEEs) are near-instantaneous disturbances characterized by the creation of a stream of electron-hole pairs in materials, resulting in unintended current flow. All of these effects are potentially catastrophic in electronic systems.

1.3.1 Total Ionizing Dose

TID effects are due to the accumulated energy deposited in a semiconductor device. TID is quantified by the unit the rad (radiation absorbed dose) or the SI unit, the gray (Gy). 1 Gy = 100 rad = 1 J/kg. Typical values for Earth-orbit satellites range from 10 krad to 100 krad over their lifetime. Most commercial electronics are not rated for this level of TID exposure. When ionizing energy is deposited into oxides, electron-hole pairs are created. The electrons are free to diffuse, but the holes travel to semiconductor-oxide interfaces where they can become trapped or begin processes that create traps. Terminal leakage currents are the most common result of TID and sometimes cause catastrophic failure in sensitive devices or at high doses. In BJTs, including SiGe HBTs, traps generated in the oxide near the base-emitter junction cause leakage current flow between the base and emitter terminals and can degrade current gain. In CMOS transistors, traps generated along the shallow-trench isolation (STI) can create parasitic channels resulting in off-state current flow, and traps generated inside the gate oxide can induce threshold voltage shifts [18].

1.3.2 Single-Event Effects

When heavy ions travel through semiconductors, they create electron-hole pairs along their path. If the path happens to encounter an electric field, like the one inside a reverse-biased PN junction, an appreciable amount of the electrons and holes are separated before they can recombine. The result is nearly instantaneous terminal

currents in the device. The umbrella term for this phenomenon is single-event effect. Three subcategories within SEEs are important to this work, single-event transients (SETs), single-event upsets (SEUs), and single-event latchup (SEL). SETs refer to the current and voltage transients that occur because of the heavy-ion strike. An SEU is specific to digital systems and is characterized by to the corruption of a digital bit, a bit flip. Finally, SEL develops when a heavy-ion strike activates latchup, the frequently catastrophic, positive-feedback mechanisms involving the runaway of the parasitic bipolar transistors present in bulk CMOS designs.

1.4 Research Objectives

The objective of this research is to investigate and establish the best practices for analog circuit design in extreme environment applications. It begins in Chapter II with the study of the use of SiGe BiCMOS technology in unshielded systems in the Lunar environment. This study developed with the block-by-block design and validation of analog and mixed-signal electronics for wide temperature ranges and radiation exposure. The chapter focuses on the design and testing of two wireline transceivers before moving on to verification of the SiGe Remote Electronics Unit. The results proved that SiGe BiCMOS technology could be used to successfully develop extreme-environment analog electronics. Chapter III focuses on effective low-noise designs in cryogenic environments. Using a cryogenic noise evaluation of IBM's 7WL SiGe BiCMOS platform, two voltage reference topologies are designed. Results from the voltage references show that the noise performance of the SiGe HBT combined with negative feedback techniques can mitigate the noise from the lower-performing devices. Next, Chapter IV includes the investigation of the single-event radiation tolerance of modern SOI CMOS platforms. Within that investigation, the single-event transients are traced, and trends of their development are found based on bias, topology, and body contacting. It is shown that transients follow the same small-signal rules used in

analog electronics and that scaling from 45 nm to 32 nm will continue to worsen the single-event response. Some best practices for body contacting and device bias are recommended. Finally, Chapter V provides a summary of the work and possibilities for future expansion.

CHAPTER II

A NEW APPROACH TO EXTREME-ENVIRONMENT SYSTEMS: SIGE BICMOS TECHNOLOGY

An enabling force behind the shift to distributed, minimally shielded electronics in extreme-environment systems is the flexibility of SiGe BiCMOS technology, specifically the SiGe HBT, to tolerate the conditions presented by extra-terrestrial environments. As the SiGe HBT is cooled to cryogenic temperatures, its most important device metrics for circuit design improve: current gain, transconductance, f_T, f_{MAX}, and broadband noise [6]. Additionally, SiGe HBTs have been shown to be robust, not only at 77 K, but also down to 300 mK [19–22]. Furthermore, high-temperature SiGe electronics have been developed. For instance, a SiGe HBT-based voltage reference has been demonstrated for operation up to 300 °C [23]. Thus, the SiGe HBT has emerged as a viable contender for ultra-wide-temperature applications.

Additionally, the SiGe HBT has a built-in resistance to TID and DD radiation effects, explained by aspects of the device structure. First, the extrinsic base of the transistor is very heavily doped. Second, the extrinsic base is located underneath an oxide/nitride composite, which is known to exhibit increased radiation immunity compared to standard oxides. In addition, the volume of the SiGe HBT is extremely small and highly doped, enhancing its hardness to DD [11]. Previous data has shown that newer generation SiGe HBT devices are hardened against major degradations in current gain in mid- and high-injection to multiple Mrad, and they have even higher TID tolerance at cryogenic temperatures [24]. Thus, the SiGe HBT thus shows great promise in being the cornerstone of extreme environment electronics as a result of its robustness against temperature variation and tolerance to radiation exposure.

In 2005, NASA began the "SiGe Integrated Electronics for Extreme Environments" project. NASA brought together six universities, four companies, and one government laboratory to develop an infrastructure to demonstrate that SiGe BiCMOS technology was a viable candidate for implementing extreme environment electronics, particularly targeting future missions to the Moon and Mars [25]. This team used the IBM SiGe 5AM process to create a library of circuit blocks of all types (analog, digital, RF, and mixed-signal) and validated them over practical lunar temperatures (−180 °C to +120 °C) and against both TID and SEL radiation effects [26, 27]. As a final proof-of-concept, the team designed and validated the SiGe Remote Electronics Unit (REU).

First inside this chapter will be a description of the REU precursor, the BAE Remote Health Node (RHN). Second, an overview of the architecture and final implementation of the REU will be described. Then, SiGe wireline transceivers designed for basic compatibility with the RS-485 and ISO 11898 standards will be presented. Lastly, a full review of the over-temperature and radiation testing of the Remote Sensor Interface (RSI) Application-specific Integrated Circuit (ASIC) with an FPGA-based implementation of the Remote Digital Control (RDC) will be covered.

2.1 BAE Remote Health Node

The SiGe REU was a miniaturized version of the key functionality of the RHN originally developed in the 1990s for the NASA X-33 space plane. The X-33 program was an experimental spacecraft for the reusable launch vehicle program. The RHN was a key component of the integrated vehicle health management (IVHM) system [28]. In the X-33 platform, the IVHM system consisted of a pair of central vehicle management computers and fifty of the RHN units distributed around the periphery of the X-33 to gather telemetry from a wide variety of sensors, as shown in Figure 5.

The RHN unit, shown in Figure 6, weighed 5 pounds, occupied a volume of just

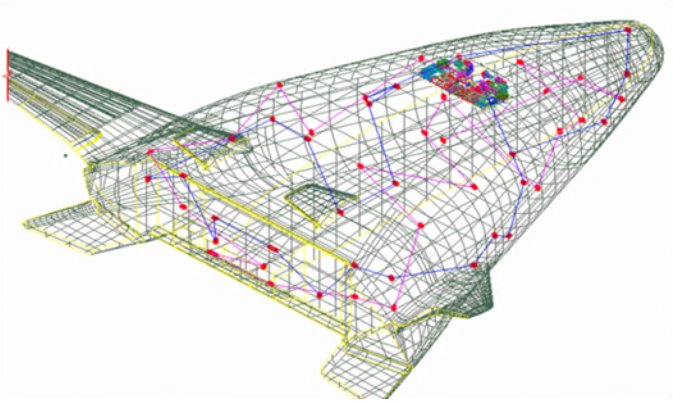


Figure 5: X-33 space plane showing distributed RHN locations [28].

over 101 cubic inches, and dissipated 17 W of power. It accepted inputs from as many as 40 sensors through several different types of processing channels via a pair of large multi-pin connectors located on one end of the box. The front-end channels were comprised of discrete analog circuits assembled into hybrid modules. Following digitization, the collected information was transmitted to the central computers via a pair of Health Optical Buses (HOB) employing the Fiber Distributed Data Interface (FDDI) protocol. Each computer supported 25 of the RHN boxes [29].

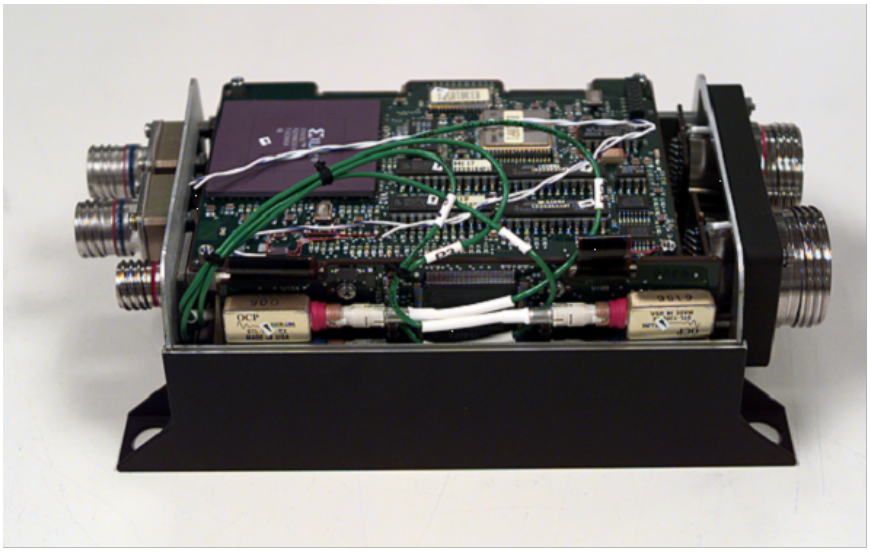


Figure 6: The original BAE Remote Health Node.

2.2 SiGe Remote Electronics Unit

The REU was designed as the combination of two ASICs, the RSI and RDC. The RSI was a consolidation of the three primary channel types from the RHN box along with analog-to-digital conversion [1, 30]. There were a total of 16 channels: 12 universal channels with selectable Wheatstone bridge inputs supporting sensors with a data rate up to approximately 200 Hz, two higher data rate (up to 5 kHz) channels each with an asymmetric bridge configuration, and two charge channels that accepted piezoelectric transducer inputs. The universal and high-speed channels incorporated custom high-voltage MOSFETs in the input stages to accommodate 12 V sensors [31]. A block diagram of the RSI is shown in Figure 7.

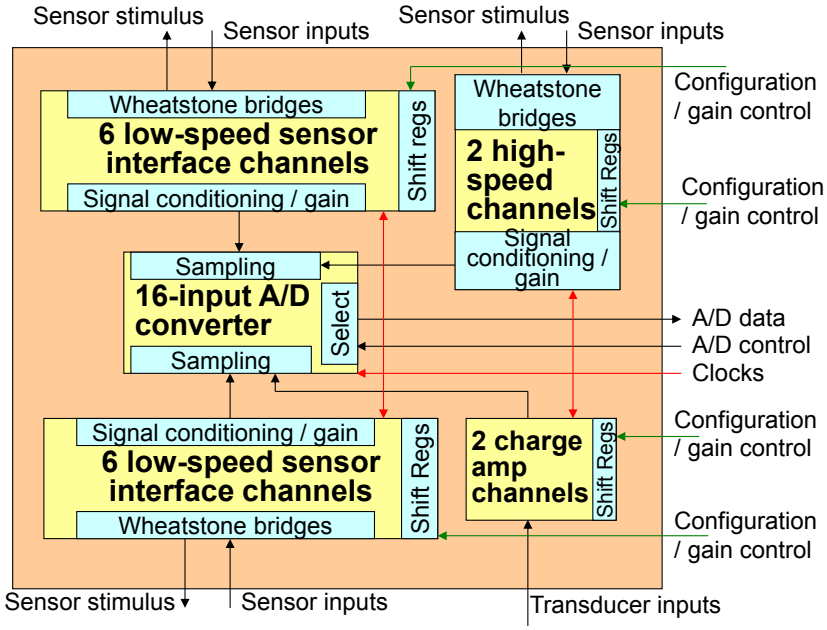


Figure 7: Simplified block diagram of the RSI ASIC [30].

Each of the channels was configured using a set of shift registers that were loaded during the initialization process and then remained static during REU operation. An additional set of shift registers fed data into the digital-to-analog converters used to calibrate the analog channels. All the registers employed radiation-hardening-by-design (RHBD) techniques to minimize the possibility of particle-induced data

corruption. Following signal conditioning in the form of bridge configuration and gain control, the analog signals were digitized in parallel using the 12-bit, Wilkinson-architecture, analog-to-digital converter (ADC) then were multiplexed in the RDC for sample averaging. A block diagram of the RDC is shown in Figure 8.

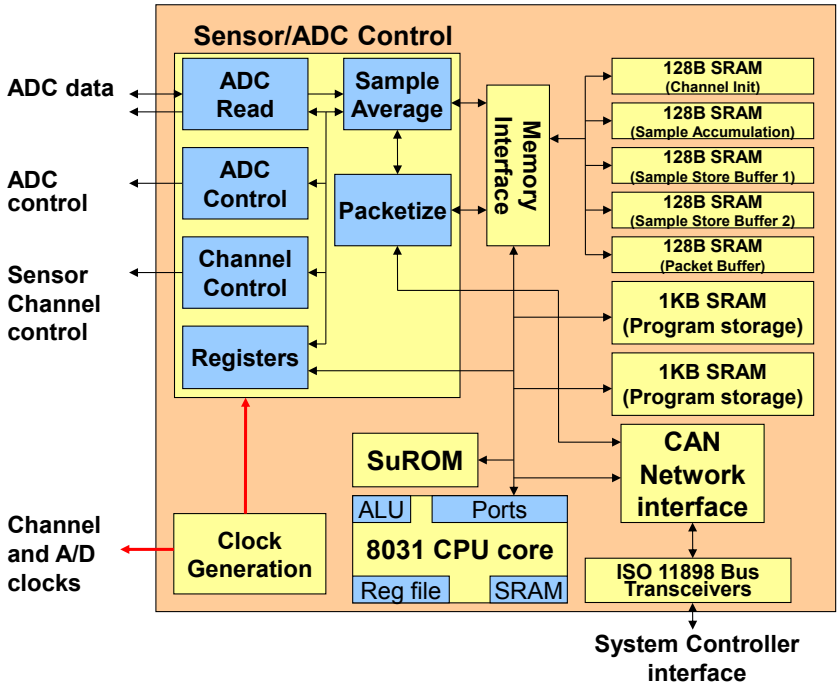


Figure 8: Simplified block diagram of the RDC ASIC [30].

The RDC was an HDL-based, CPU and finite-state machine (FSM) driven system that read, processed, and sent the samples from the RSI chip to a central system via the controller area network (CAN) bus over an ISO 11898 physical layer. In addition to the CPU and CAN circuits, the RDC contained register-configurable FSMs for CAN packet building and RSI sample processing and storage elements for CPU instructions, processed samples, and configuration data for all 16 RSI channels.

The RDC followed a sequence of operations divided into the start-up and execution phases. After power-up and reset, it went into start-up where it set up the CAN bus interface and broadcast a message to all other CAN bus devices, including the system controller, to indicate its presence on the bus. The system controller then

sent commands over the CAN bus, programming the 8031 for execution and selecting values for the RSI channel settings.

During execution, the RDC sent control signals to the RSI control interfaces and received raw digital samples from each of the 16 channels through the ADC. FSMs then process the samples on a per-channel basis as shown in Figure 9. An accumulation filter selected which ratio of samples to save based on the programmed sample rate for that channel. For example, a 1:8 accumulation ratio meant for every eight raw samples received from a channel, one would be kept and seven would be ignored. In this way, the CAN bus was not over-crowded with unnecessary data.

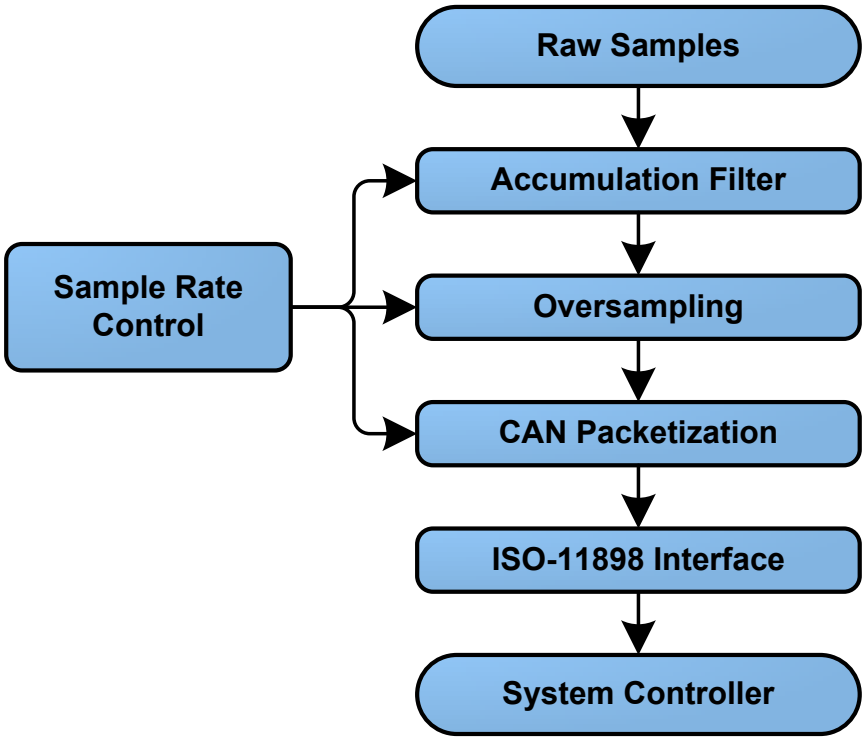


Figure 9: Simplified flow diagram of the RDC operations.

The selected raw samples converged in oversampling, the next stage of the sample pipeline. Here, samples were averaged together based on a given over-sample ratio that was also defined by the sample rate of each channel. As a second example, a 32:1 over-sample ratio meant 32 raw samples were used to produce an averaged sample. Next, an FSM built the averaged samples into CAN data packets for eventual

transmission to the system controller. Once ready, those packets were transmitted over the CAN bus to the system controller via the ISO 11898 physical layer. A diagram of the final envisioned implementation of the REUs is shown in Figure 10.

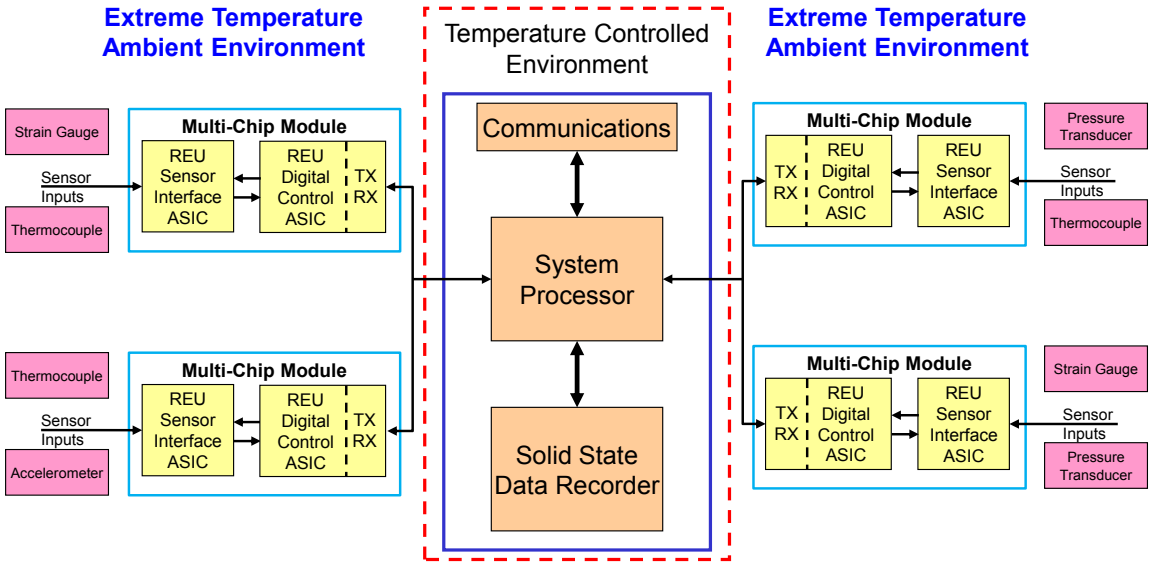


Figure 10: Block diagram of the envisioned implementation of the REUs.

2.3 Cold-capable, Radiation-hardened SiGe BiCMOS Wireline Transceivers

Within the RDC were transceivers that enabled communication to the system controller. At the end of the project, the ISO 11898 communication standard was chosen, but earlier the RS-485 standard was selected. This work improves the RS-485 transceivers presented in [32] and introduces the ISO 11898 transceivers designed for the final implementation of the REU [3, 4].

2.3.1 RS-485 Transceiver

2.3.1.1 Transmitter Design

The RS-485 transmitter takes in a single-ended 3.3 V CMOS digital signal and translates it to a differential bus signal. The input signal is gated for an enable/disable operation then buffered to drive subsequent stages. An example RS-485 bus is shown

in Figure 11 [32]. The output utilizes a BiCMOS gate topology for output drive capability as shown in Figure 12. A resistor is used to prevent current peaking in the lower 32 parallel HBTs improving the long-term reliability of the transmitter. Ballast resistors on the emitters of the upper HBTs serve to maintain even current density through each of the 32 parallel HBT-with-resistor structures. Two such output stages are required, one for each side of the differential bus.

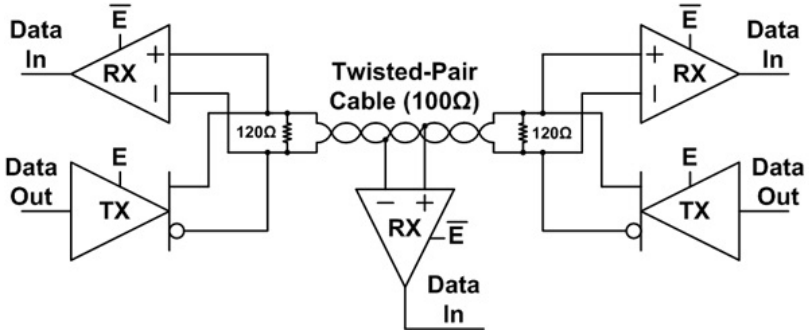


Figure 11: Example block diagram of an RS-485 bus with multiple transceivers [32].

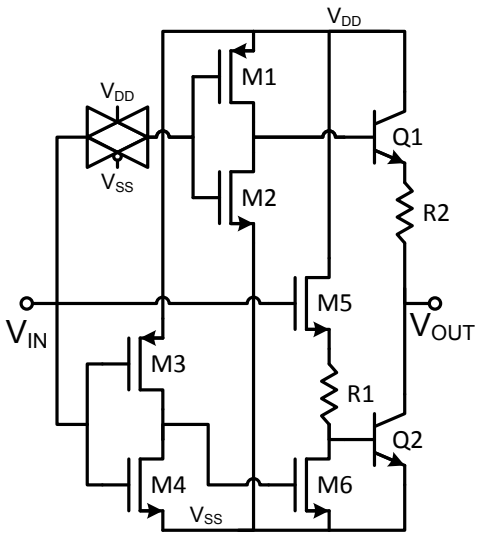


Figure 12: Schematic of the RS-485 transmitter output stage. Two such output stages are used, one for each side of the differential bus.

2.3.1.2 Receiver Design

The receiver converts the differential bus signal back to a 3.3 V CMOS digital signal. Resistor networks at the inputs serve to improve the input common-mode range as shown in Figure 13. They are weighted in the positive direction to align with the n-type input differential pair. They are followed by active loads that wrap the signal around for rail-to-rail range into CMOS inverters that buffer the signal to the output. Hysteresis is provided by a polysilicon feedback resistance from the output of the differential pair back to base terminal of the positive side of the differential pair.

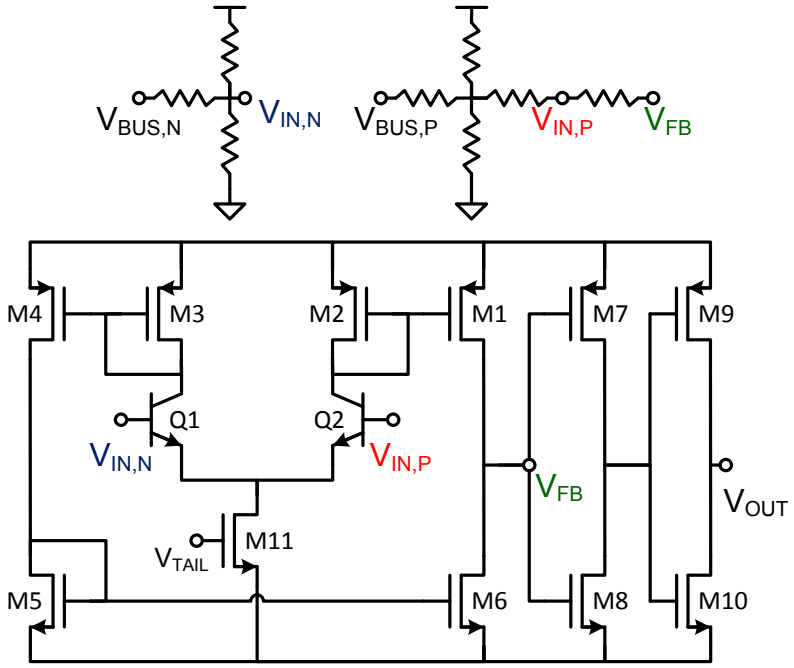


Figure 13: Schematic of the RS-485 receiver core. The input resistor networks extend the common-mode range outside the positive and negative rails.

2.3.1.3 Measurement Results

The transceivers were wirebond packaged inside 28-pin dual in-line packages (DIPs) in pairs because each one can only be enabled as either a transmitter or receiver. The room-temperature measurement shown in Figure 14 required high-speed, screw-on, low-loss SubMiniature version A (SMA) connectors to maximize the measurement

bandwidth. The SMAs were connected through bias tees to the 50 Ω, high-speed oscilloscope ports on a Tektronix DPO71254. The transceivers performed robustly at 20 Mbps.

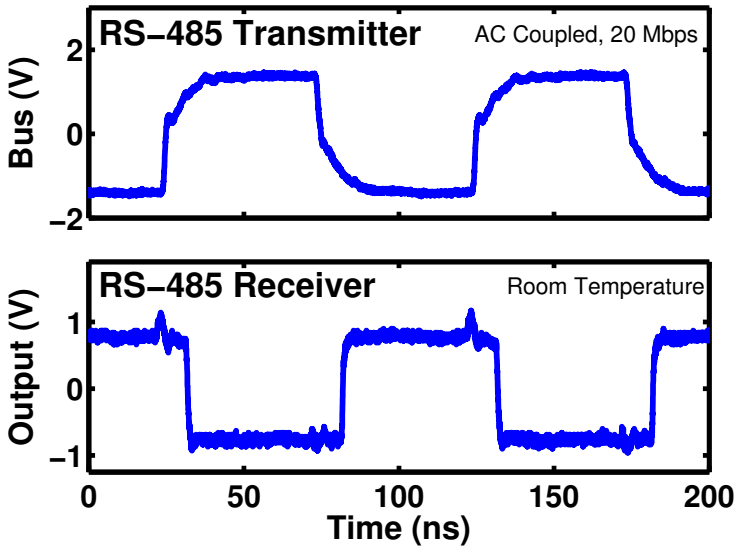


Figure 14: Oscilloscope capture of two RS-485 transceivers operating concurrently at a data rate of 20 Mbps. One transceiver is enabled as the transmitter and the other as the receiver.

Other DIPs were tested inside a cryogenic dewar with coaxial conductors from 90 K up to 390 K with 50 K steps. One bus termination was located as close as possible to the transceiver, just outside the dewar, and the other was placed near the oscilloscope for signal integrity. The bandwidth of the dewar limited the over-temperature measurements to a speed of 2 Mbps. Measurements were made with a Tektronix AFG3252 function generator and a Tektronix TDS7054 oscilloscope using the oscilloscopes built-in measurements of rise/fall time, propagation delay, and signal amplitude. Figure 15 shows the propagation delay of the receiver and transmitter over temperature. The receiver was largely unchanged while the transmitter saw an improvement of about 2 ns at the lower temperature points.

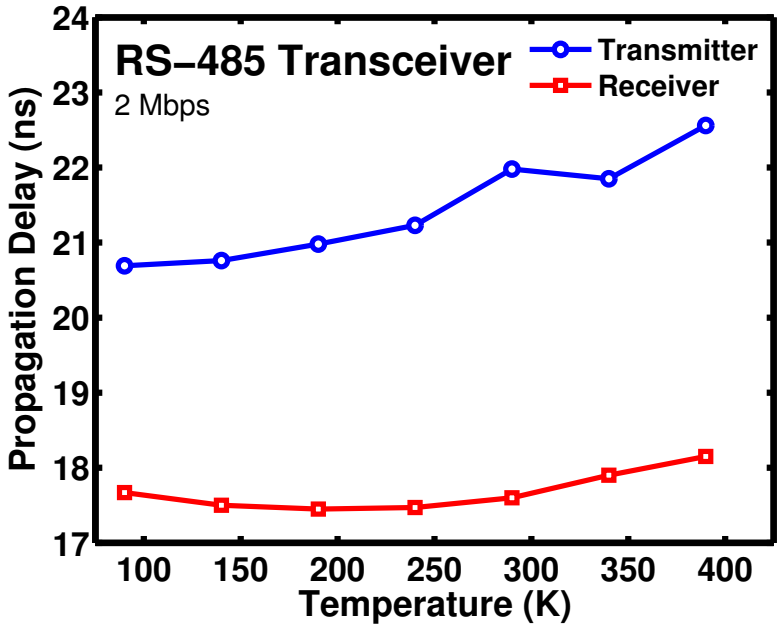


Figure 15: Propagation delay for the RS-485 transmitter and receiver operating at 2 Mbps over a 300 K temperature range. The receiver propagation stays relatively flat while the transmitter gets faster at lower temperatures.

Receiver The receiver hysteresis was measured with an HP 4155 sweeping the positive side of the bus while holding the negative side at ground. The results are shown in Figure 16. The hysteresis range monotonically decreases as temperature rises due to the temperature drift of the input and feedback resistor network.

Transmitter Figure 17 shows the rise and fall time of the transmitter over temperature. The values tended to stay constant through most of the range except for one outlier in the fall time. Close to the upper bound, the values began to increase as the output transistor slowed. The measured output swing is shown in Figure 18. The dip at bottom of the temperature range is the result of the VBE shift due to presence of fewer thermally activated carriers. The total change in swing is less than 150 mV or 5% of the average.

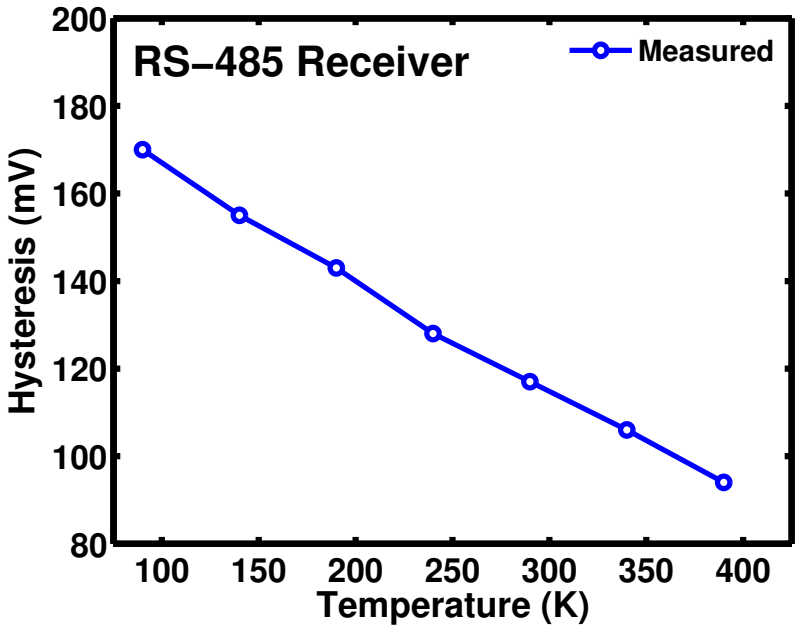


Figure 16: Hysteresis range for the RS-485 receiver operating over a 300 K temperature range. The change is due to the temperature drift of the resistance of the polysilicon on deep trench resistors used in the input and feedback network.

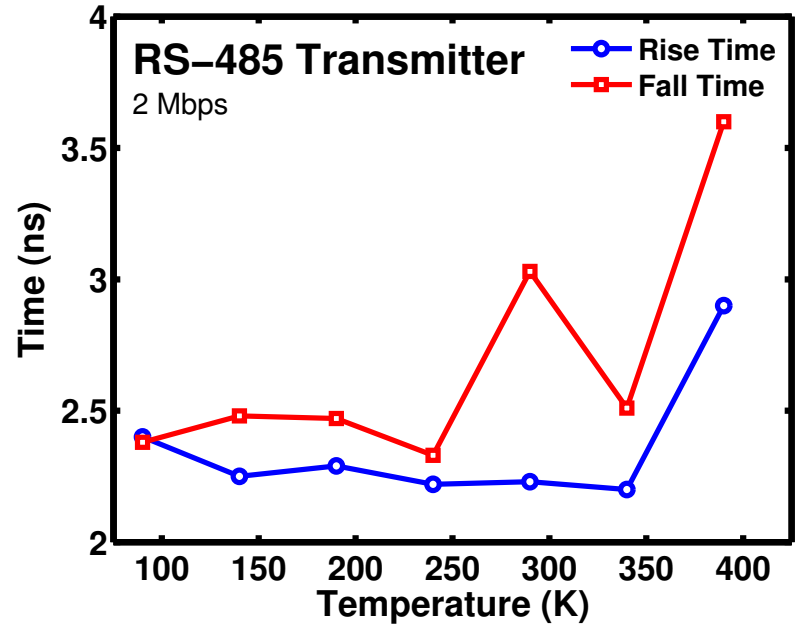


Figure 17: Rise and fall times for the RS-485 transmitter. Values tend to stay constant for most of the temperature range with one outlier in the fall time. As the temperature nears 400 K the output transistors tend to slow and the times increase.

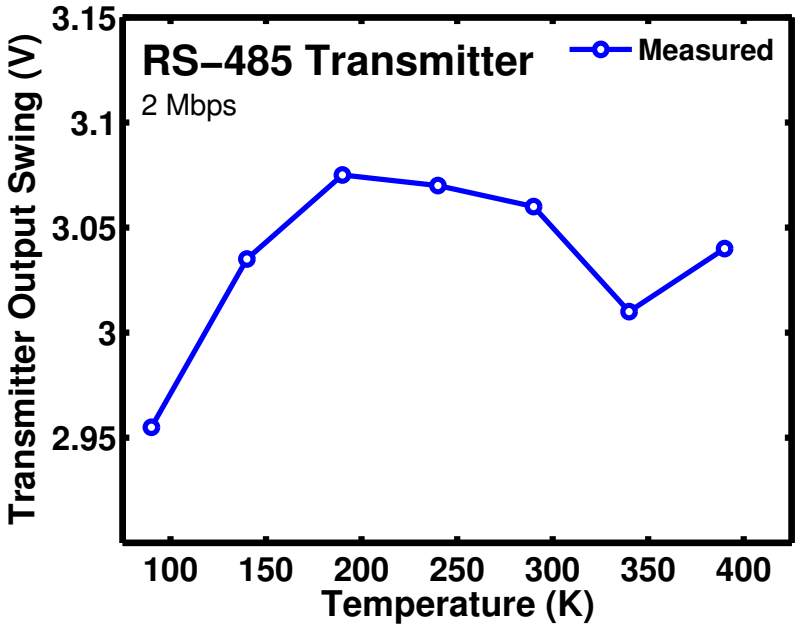


Figure 18: The output swing of the RS-485 transmitter varied less than 150 mV across the entire temperature range. The drop at lower temperatures is due to the larger required VBE by the top device.

2.3.1.4 RS-485 Die Photo and Performance Summary

A die photo of the RS-485 transceiver is shown in Figure 19. It only occupies 575 μm x 375 μm of space without pads, which is less than 0.25 mm^2. A number of RS-485 transceiver performance parameters are shown in Table 1.

Table 1: RS-485 Transceiver Performance

Specification	Value
Transceiver Max. Data Rate	$>$ 20 Mbps
Receiver Propagation Delay	$<$ 19 ns
Receiver Hysteresis Range	$>$ 90 mV
Receiver Current Consumption	$<$ 3 mA
Transmitter Propagation Delay	$<$ 23 ns
Transmitter Rise/Fall Time	$<$ 4 ns
Transmitter Output Swing	$>$ 2.9 V
Transmitter Current Consumption	$<$ 53 mA

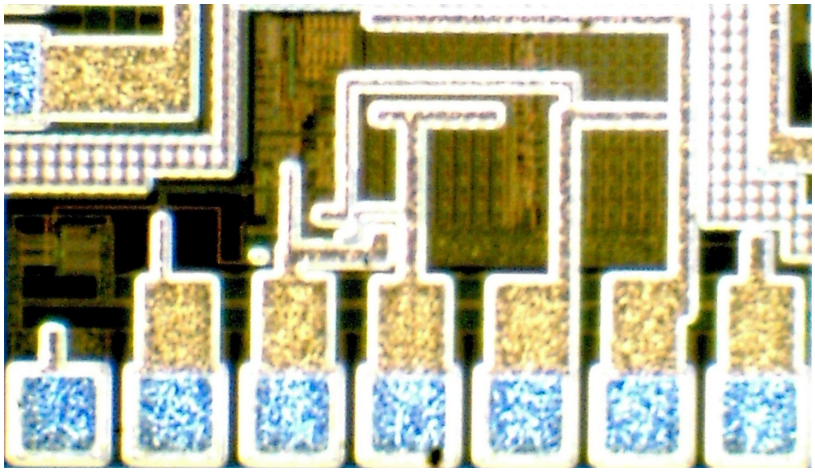


Figure 19: Die photo of the RS-485 transceiver. It only occupies about 575 μm x 315 μm without pads.

2.3.2 ISO 11898 Transceiver

2.3.2.1 Transmitter Design

The input stage of the ISO 11898 transmitter uses combinational logic rather than transmission gates to implement the enable/disable functionality. The change reduces the transmitter propagation delay and makes it simple to implement the high-impedance recessive state. The necessary data inversion compared to the RS-485 transmitter also takes place in the combinational logic.

The dominant '0' condition of the ISO 11898 standard (dominant positive voltage on the bus itself) simplifies the output stage shown in Figure 20. Each side of the differential bus is only required to provide voltage/current drive in one direction, asserted only during the dominant condition. When recessive, the output presents a high impedance value. This implementation looks similar to the RS-485, but the output is split such that the positive side of the bus is only connected to the emitter ballast of the upper HBT array and the negative side of the bus is only connected to the collector of the lower HBT array. As with the RS-485 each HBT represents 32 devices. The bottom 32 devices share all nets. The devices in the top array share base and collector nets, but each has their own emitter ballast resistor that then shares

the positive bus net.

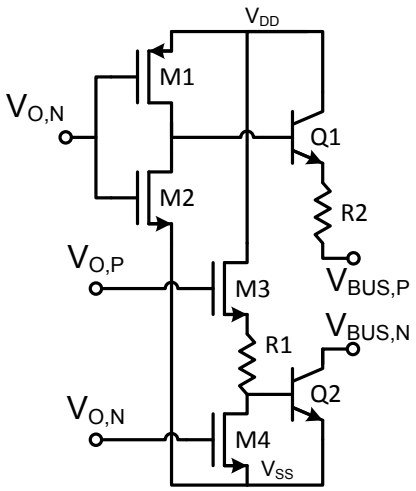


Figure 20: Schematic of the output stage of the ISO 11898 transmitter. Because it only provides drive in one direction, only one such stage is needed.

2.3.2.2 Receiver Design

The ISO 11898 receiver has a resistor-network input similar to the RS-485. Resistor value differences between the positive and negative differential inputs move the decision point from 0 V to between 500 and 700 mV to be compatible with the ISO 11898 standard. Additionally, the input sides are swapped to implement the data inversion from the bus.

2.3.2.3 Over-temperature Measurement

The same over-temperature setup for the RS-485 was used for the ISO 11898 transceiver measurements. The hardware was at temperature in the dewar, but the data bus and terminations were at room temperature outside the dewar. Propagation delay was measured by passing data through the transmitter, onto the bus, and back through the receiver. Both the bus and the receiver output were monitored. Figure 21 displays the measured values of propagation delay over temperature through the transmitter only and the transmitter and receiver together. This data representation adds the offset caused by the internal dewar cabling equally to both values. There was less

than a 4 ns difference from the highest to the lowest temperature point caused by the increased speed of the devices at low temperatures.

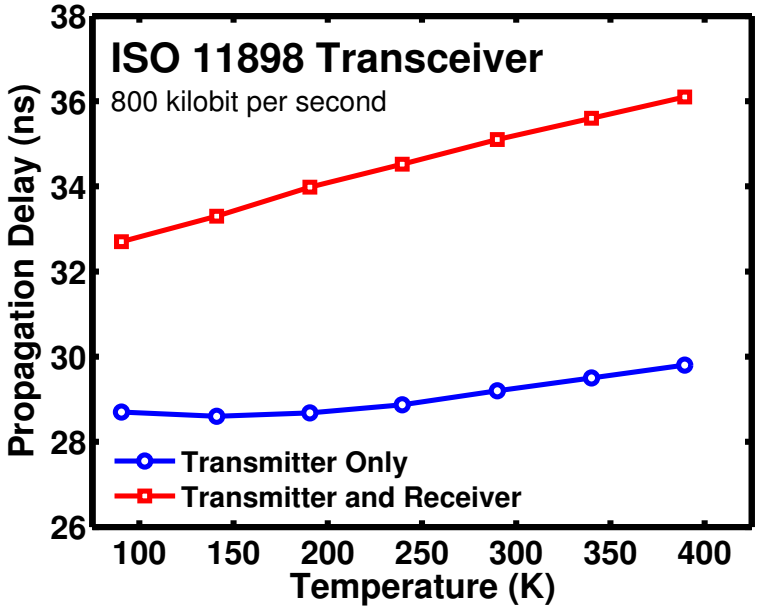


Figure 21: The ISO 11898 transceiver propagation delay is consistent over temperature, showing an approximate 3 ns change from the highest to lowest points.

Receiver The ISO 11898 receiver hysteresis was measured with an HP 4155 sweeping the positive side of the bus while holding the negative side at ground. The results are shown in Figure 22. Much like the RS-485, the hysteresis range monotonically decreases as temperature rises due to the temperature drift of the input and feedback resistor network. All values are acceptable for the final implementation of the receiver.

Transmitter The rise and fall times of the transmitter output are shown in Figure 23. They are dominated by the parasitic capacitance seen by the bus and are very consistent over temperature, varying less than 1 ns. Experiments were also conducted over cable length. The resulting rise time measurements are shown in Figure 24. Even over the 50 ft. bus, rise times were consistent across transmitter temperature, never

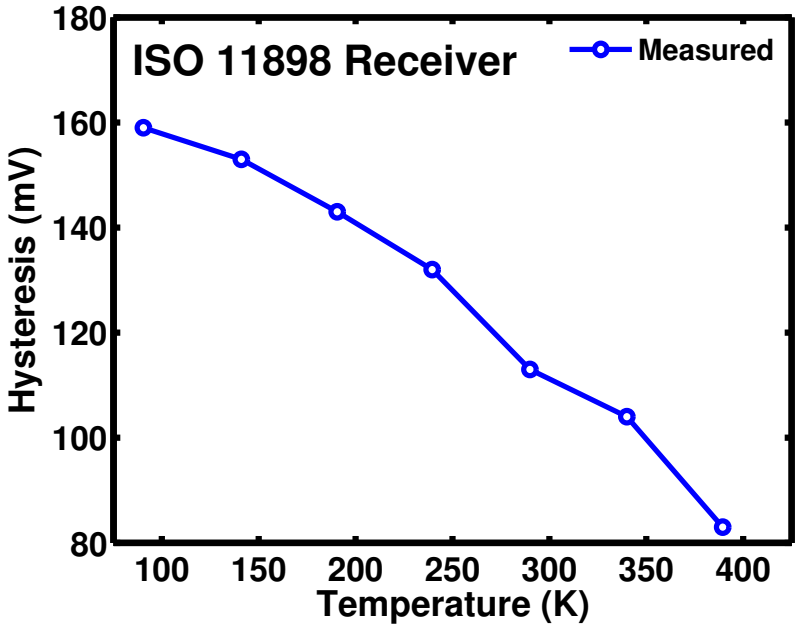


Figure 22: Hysteresis range for the ISO 11898 receiver operating over a 300 K temperature range. The change is due to the temperature drift of the resistance of the polysilicon on deep trench resistors used in the input and feedback network.

changing more than 0.5 ns.

Finally, the output swing is shown in Figure 25. The output swing decreases by approximately 0.5 V over temperature from the increased VBE requirement of the output SiGe HBTs at lower temperatures. The overall value is lower than the RS-485 because of the unidirectional drive.

2.3.2.4 Total Ionizing Dose Experiment

The total ionizing dose test was conducted at Crocker Nuclear Laboratory at the University of California, Davis [33]. Hardware was irradiated with 63 MeV protons to three levels: 200 krad(SiO_2), 500 krad(SiO_2), and 2 Mrad(SiO_2). Samples were wire bonded into a DIP, soldered onto a printed circuit board and clamped in the beam line as shown in Figure 26. At each dose level, samples were removed from the fixture, tested, and returned for further irradiation.

Measurements were performed with a Tektronix AFG3252 function generator and

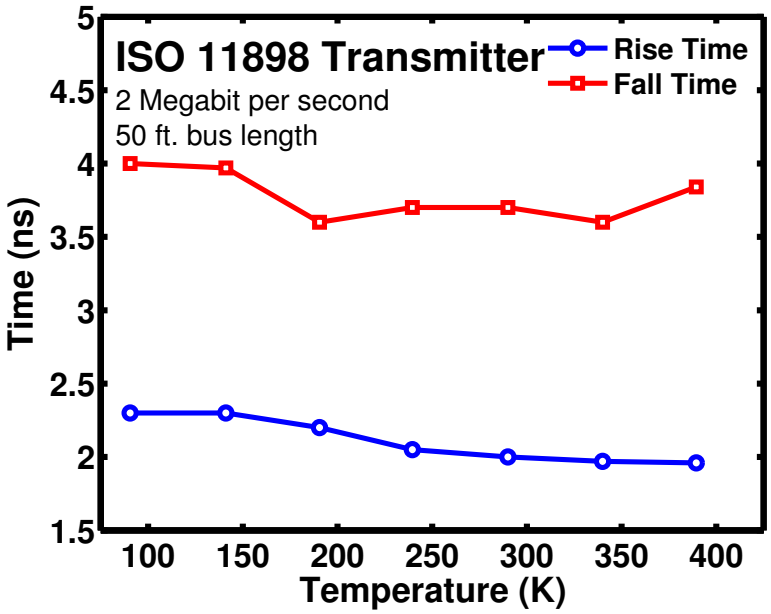


Figure 23: The rise and fall times of the ISO 11898 transmitter vary minimally over temperature, helping to ensure robust transition edges throughout the range.

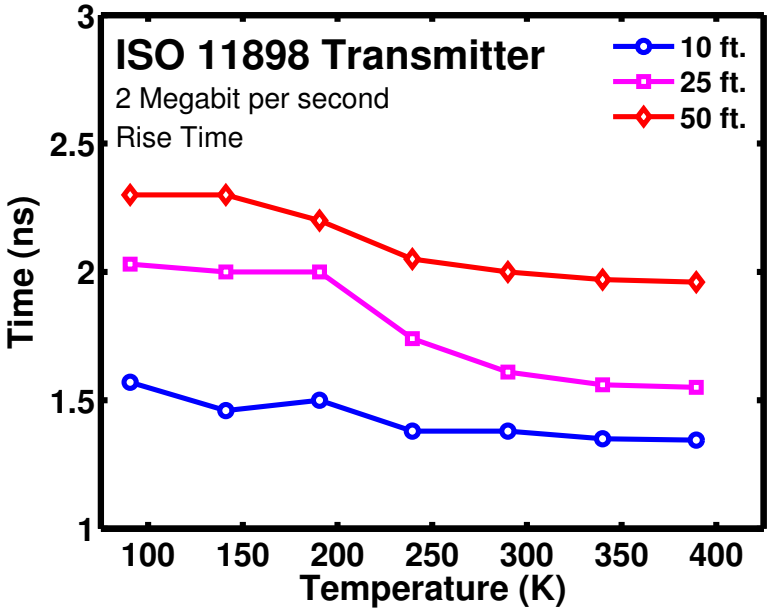


Figure 24: The rise time of the ISO 11898 is nearly constant over temperature with various bus lengths.

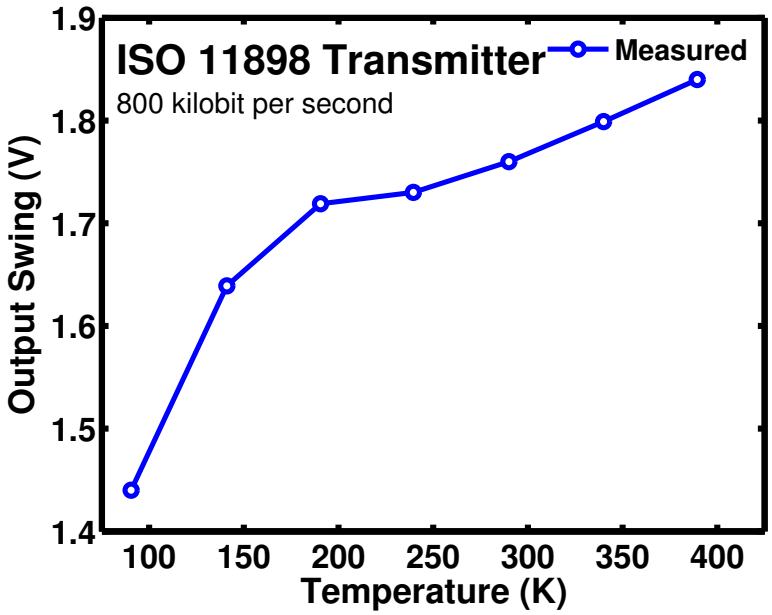


Figure 25: The output voltage swing of the ISO 11898 increases over temperature. It is approximately 1 V lower than the RS-485 because of the unidirectional current drive.

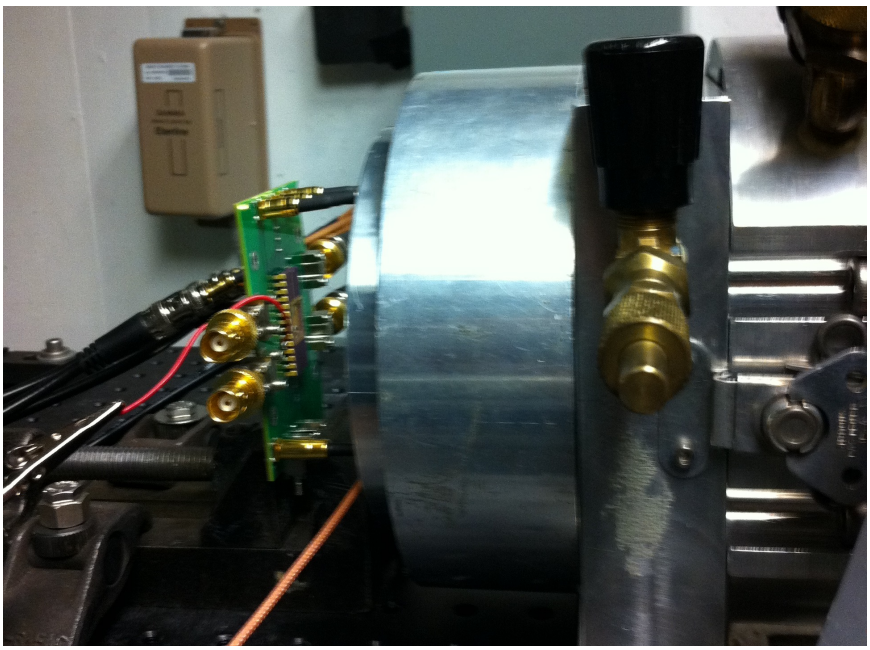


Figure 26: Photograph of the ISO 11898 transceiver sample setup for proton irradiation at Crocker Nuclear Laboratory.

a Tektronix TDS2012B oscilloscope. Much like the over-temperature measurement, propagation delay was measured from the transmitter input to the bus, and from the transmitter input to the receiver output. Both the receiver and transmitter showed radiation hardness through 2 Mrad(SiO_2) dose. Most of the measured specifications stayed within 5 % of their pre-rad values. Even the transmitter falling-edge to rising-edge propagation delay, which changed the most, varied less than 15 % from nominal. The average percent changes of output swing and propagation delays are shown in Figure 27.

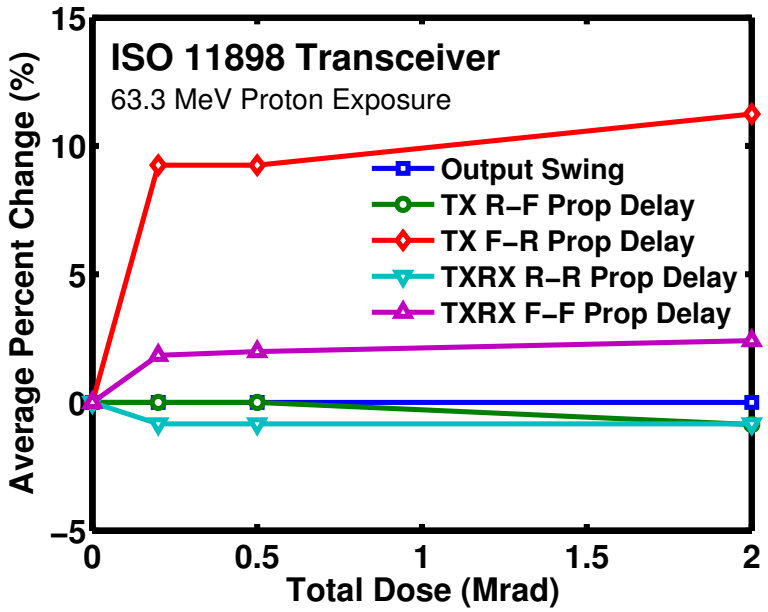


Figure 27: Percent change for various transceiver parameters versus total ionizing dose. The ISO 11898 transceiver is shown to be TID tolerant to 2 Mrad. Most parameters stay within 5 % of their pre-rad values. The largest change stays within 15 %.

As a secondary check to the measured data, compact-model simulations were executed with empirical TID models. Device TID data provided by [24, 34, 35] were utilized to calibrate leakage current sources implemented in Verilog-A for circuit simulation, as shown in Figure 28. Simulations modeled worst-case 540 krad radiation exposure of the nFETs and 1 Mrad exposure of the SiGe HBTs. Results showed

similar trends as those seen in measurement. The measured and simulated changes are shown in Table 2. Measurable changes were in the same direction as simulation, and immeasurable changes were confirmed to be minimal in simulation.

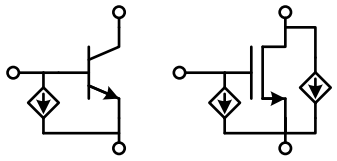


Figure 28: The basic form of the empirical models used for simulation of TID damage to the transceiver.

Table 2: ISO 11898 Measured vs. Simulated Total Ionizing Dose Changes near 500 krad(SiO_2)

Specification	**Meas.**	**Sim.**
TX Output Swing	0.0 V	0.01 V
TX R-F Propagation Delay	0.0 ns	−0.03 ns
TX F-R Propagation Delay	0.9 ns	0.09 ns
TXRX R-R Propagation Delay	0.0 ns	−0.05 ns
TXRX F-F Propagation Delay	0.4 ns	0.67 ns

2.3.2.5 Broad-beam Testing

The broad-beam heavy-ion experiment took place at Lawrence Berkeley National Laboratorys Berkeley Accelerator Space Effects Facility. Three ion species from the 10 MeV/nuc cocktail were used: O, Cu, and Xe. The resulting surface linear energy transfer (LET) values and approximate deposited charge along the ion path are shown in Table 3. A normal angle of incidence was used for all three ions. Xenon was the highest LET ion available in the cocktail and represents the practical worst-case in heavy-ion-strike testing. Xenon strikes are extremely rare in actual space environments. For this experimental setup, the circuit was wire-bonded onto a PCB that was mounted in the vacuum chamber in the beam line. Transient measurements were done with a Tektronix AFG3252 function generator and a Tektronix DPO71254 high-speed oscilloscope with attached bias tees on the inputs to block the DC levels.

Table 3: Heavy Ions in Broad-beam Testing

Ion	**Surface LET ($MeV \cdot cm^2/mg$)**	**Approx. Deposited Charge ($pC/\mu m$)**
Oxygen	2.19	0.023
Copper	21.17	0.218
Xenon	58.78	0.606

For the receiver tests, the negative side of the bus was grounded; the positive side was stimulated with a 1 MHz square wave, and the receiver output was monitored. The receiver exhibited numerous transients during Xe bombardment. Most transients peaked at the opposite output rail; i.e., when the output was at the '0' voltage level, the transient voltage peak would be at the '1' level and vice versa. An example is shown in Figure 29. This transient signature can be indicative of a sensitive CMOS inverter. Concordantly, the receiver output is buffered by a pair of CMOS inverters with large aspect ratios designed to drive the output pad. These devices are the largest in the receiver. It is reasonable to theorize that these inverters account for the most sensitive area in the receiver. In the final application, they will not be present, as the receiver output will be used by other on-chip circuitry, so in end-use conditions, the receiver could have notably higher tolerance to single-event effects. More investigation is needed to verify this claim.//

During the transmitter tests, the transmitter input was stimulated with a 1 MHz square wave, and each side of the data bus was monitored separately. The shunt 50 Ω oscilloscope impedance on each side of the data bus caused excessive over- and under-shoot of the transmitter signal switching to the high-impedance recessive bus state. It limited the minimum detectable transient in that state to 320 mV over-shooting the steady-state value or 130 mV under-shooting it on each side of the differential bus. It should be noted that transients below this threshold would not result in data disruption in the ISO 11898 communication standard. Switching to the dominate state was unaffected.// The transmitter proved to be tolerant against single-event

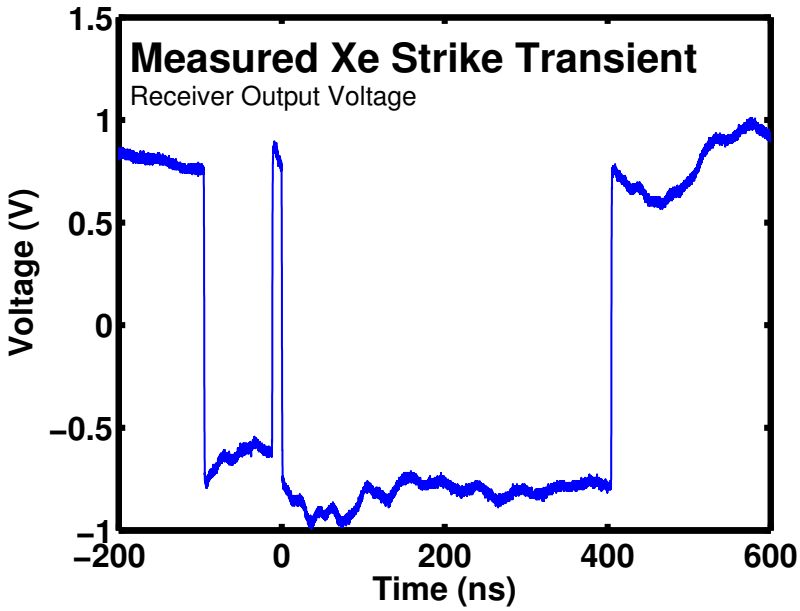


Figure 29: A measurement of a typical Xe strike of the ISO 11898 receiver. The strike results in a transient pulse with a peak on the opposite rail, possibly indicative of a CMOS inverter. The large buffers driving the output pad are theorized to be responsible for these transients.

transients. Irradiation with O ions produced no measurable transients on the data bus in either state. Cu and Xe ions did produce measurable transients on the single-ended bus voltages; however, the transients had minimal effect on the differential bus voltage. Figure 30 shows a typical transmitter transient from the highest LET ion, Xe. The resulting transient results in an almost purely common-mode signal that would be rejected by receivers on the bus. The differential component peaks at 56 mV, over an order of magnitude lower than the voltage necessary to cause an upset.

2.3.2.6 Technology Computer-Aided Design Simulations

Technology Computer-Aided Design (TCAD) simulations were used to confirm the broad-beam results. A 3-dimensional TCAD model of the IBM 5AM SiGe HBT was developed and is shown in Figure 31. The model was calibrated to the devices of the same size as those used in the transmitter. Simulations modeled a Xe ion strike into

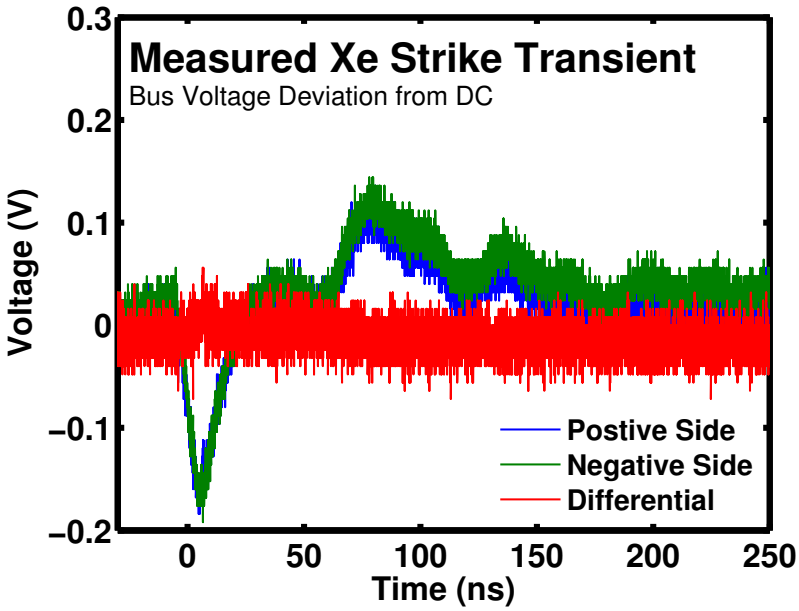


Figure 30: A measurement of a typical Xe strike of the ISO 11898 transmitter. The strike results in a signal with a mostly common-mode component. Neither the common-mode nor the differential component is large enough to disrupt data on an ISO 11898 bus.

the center of the emitter stack of the device at the four unique bias points expected in the transmitter. The results of one of the simulations are shown in Figure 32. As is normal, the collector and emitter currents were the largest and exhibited opposite polarity. These simulated strike currents were then used in corresponding current injection simulations of the transceiver.

To execute the current injection simulations, ideal current sources referencing the results of the TCAD simulations were placed between the terminals of a transistor to mimic the effects of a strike on that device. The simulation setups covered strikes on each of the two transmitter output devices at each of the two circuit states. The differential bus voltage variation from each of the four situations can be seen in Figure 33.

The simulations confirmed the broad-beam measurement result: the ion strikes result only in non-disruptive signals. In all cases, the differential transients have

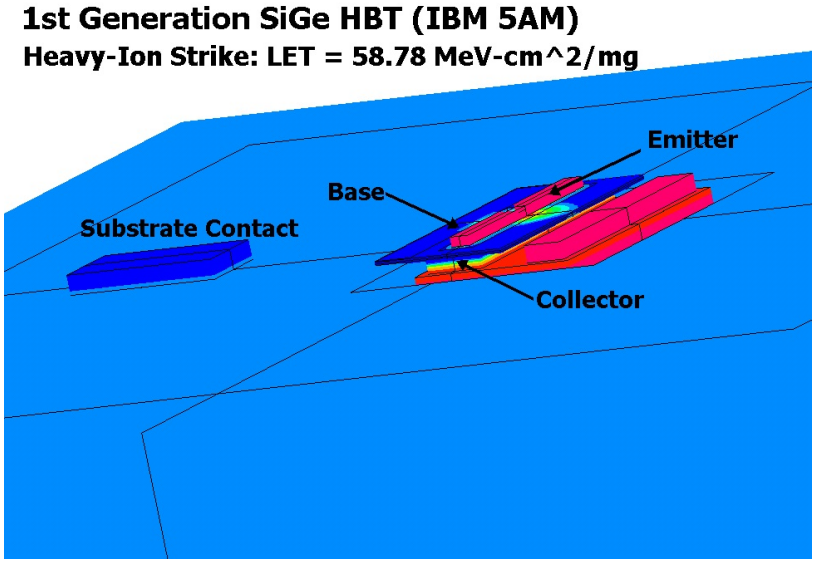


Figure 31: The three-dimentional TCAD model of the SiGe HBT used for strike simulations. It was calibrated to match devices of the same size as those in the transmitter.

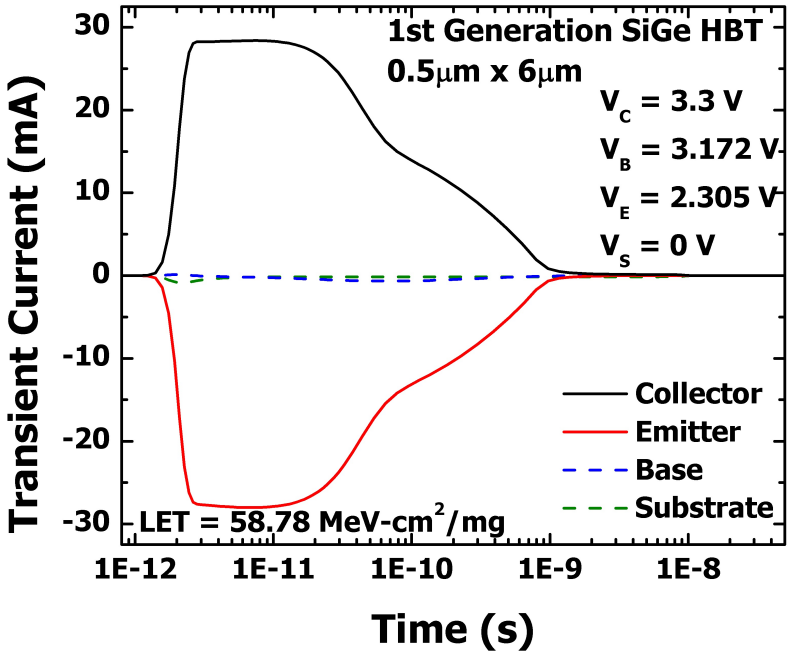


Figure 32: The results of one of the four 3-D TCAD simulations of the currents from a Xe strike with a constant 58.78 MeV·cm^2/mg LET in the emitter stack of a 0.5 μm x 6 μm SiGe HBT. Simulated currents were used in the current injection simulations.

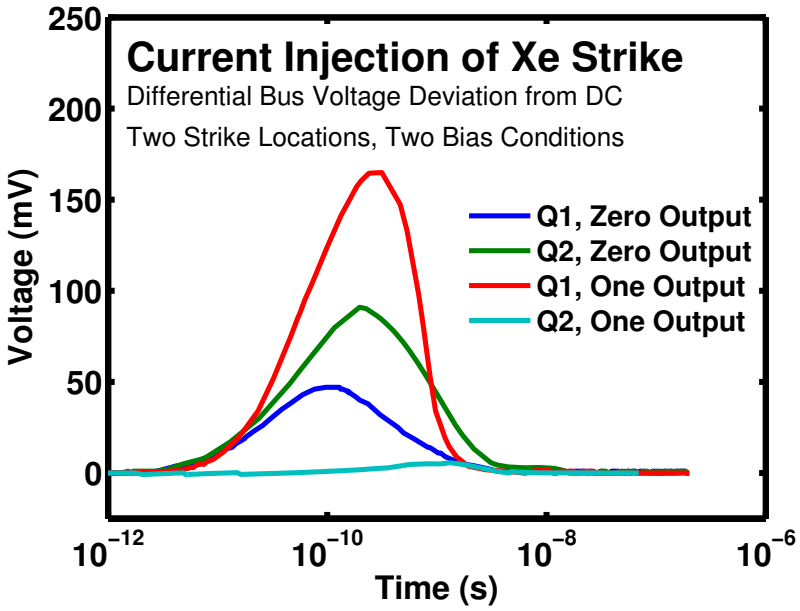


Figure 33: Current injection simulations of a Xe strike in the output stage of the ISO 11898 transmitter. In all cases, strikes result in signals with a minimal differential component, too small to disrupt data on an ISO 11898 bus.

positive peaks, which would have no effect in the case of a '1' output from the transmitter because the differential voltage would already be positive. In the cases where the transmitter has a '0' output, the maximum differential peak is less than 100 mV, approximately an order of magnitude less than the necessary swing to cause a data transition (bit upset). The transmitter is shown to be hardened against these single-event effects even at LETs near 60 MeV·cm^2/mg.

2.3.2.7 ISO 11898 Chip Overview

A die photo of the ISO 11898 transmitter is shown in Figure 34. It only occupies 320 μm x 330 μm of space without pads, which is less than 0.110 mm^2.

2.3.3 Overview

This work presented the design and testing of two SiGe BiCMOS wireline transceivers enabling a part of the new distributed system perspective by creating a means of control and communication across vehicle-wide buses. Both the RS-485 and ISO

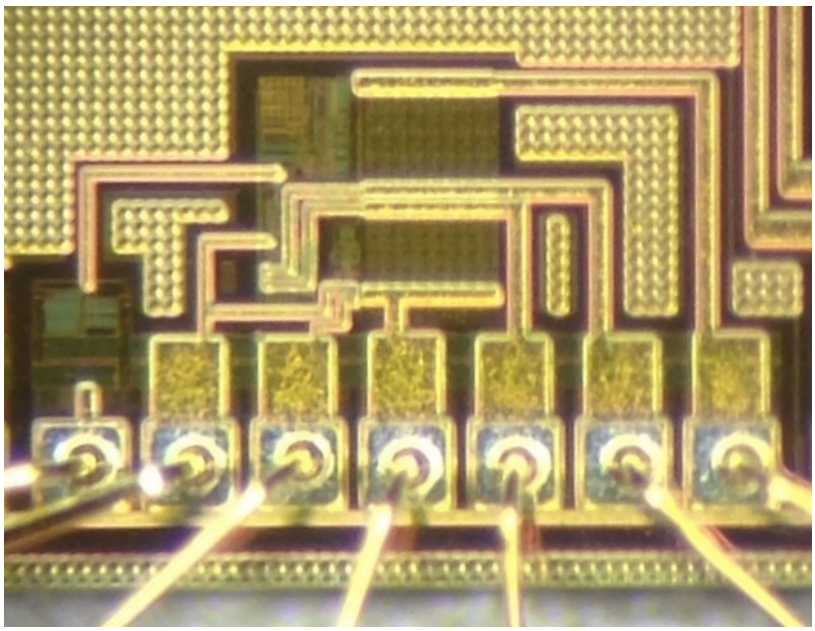


Figure 34: Die photo of the ISO 11898 transmitter wire- bonded for over-temperature measurements. It only occupies 320 μm x 330 μm without pads.

11898 transceivers were shown to work robustly from 90 K to 390 K, with consistent rise/fall times, propagation delays, and output amplitudes. Additionally, the ISO 11898 transceiver was TID tolerant to 2 Mrad, and the transmitter was hardened to single-event effects. This work added a piece to the distributed electronics puzzle by facilitating robust communication throughout space-based systems with minimal temperature control and radiation shielding.

2.4 RSI-with-FPGA Remote Electronics Unit

Due to the unavailability of the RDC ASIC, final measurement of the REU took place with the RSI ASIC paired with an FPGA implementation of the RDC. Much of the same HDL code used in the RDC design flow was used to program the FPGA.

2.4.1 Wide Temperature Testing

2.4.1.1 Over-temperature and Radiation Test Dewar

A cryogenic dewar customized for single-event testing [36] was used for carrying out the over-temperature and single-event radiation experiments. It is shown in Figure 35.

The dewar could be used with LN_2 (boiling point 196 °C) or LHe (boiling point 269 °C) as cryogens, depending upon the lowest temperature desired. Six hermetically sealed ports on the dewar provided ample choice for a variety of electrical connection configurations, such as hermetic 61-pin connectors for dc measurements or customized hermetic high speed feedthroughs for transient capture [36]. Two of these ports were fitted with customized vacuum-sealed flanges, each mounted with multiple 25-pin electrical micro-D subminiature (MDM) feedthroughs. A mechanical heat switch enabled control over the amount of heat transfer between the dewar/DUT and the external world.

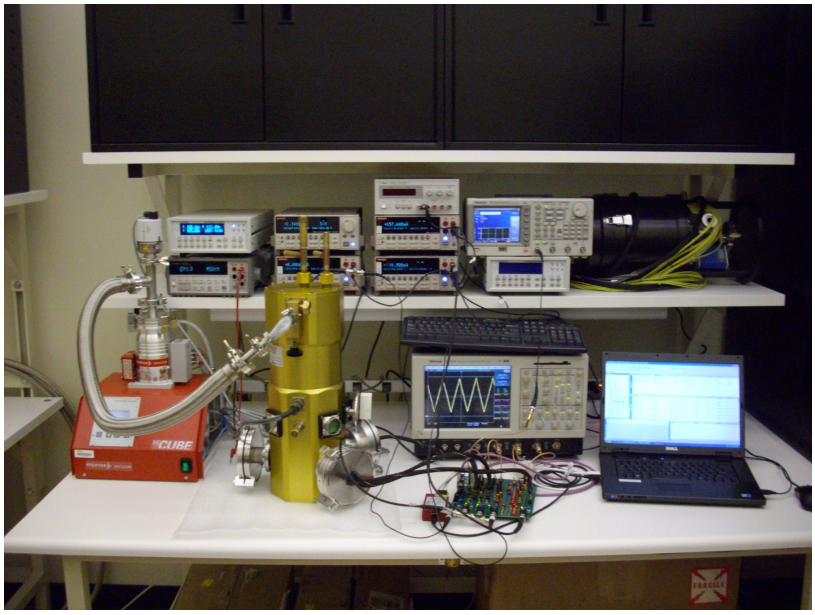


Figure 35: The over-temperature experimental set-up.

The beam port of the dewar was flange adaptable to match that of the broad beam line at the test facility, the Texas A&M University Cyclotron Institute. The dewar beam port was adapted with a hermetically sealed Aramica window flange similar to the one on the beam line. The RSI test board was designed such that the center of the DUT corresponded to the central axis of the beam line.

The DUT was cooled using a custom-designed copper cold finger that was in contact with both the DUT and the dewar cryogen vessel. Temperature sensors were placed

on the cold finger and the dewar vessel to monitor the respective temperatures simultaneously through an external Lakeshore 331S temperature controller. The controller was used to regulate the heat applied to the system through a 50 W heater attached to the dewar vessel, and thus facilitated single-event testing over temperature.

2.4.1.2 Test Board Design

Test board design for the RSI was constrained primarily by the radiation test dewar. A two-board solution was chosen with the goal of keeping the maximum amount of the supporting commercial circuitry at room temperature. The in-dewar daughter card held the RSI and FPGA-based RDC. Outside the dewar, the motherboard contained all the power management and interface circuitry.

Daughter Card The internal volume of the test dewar and availability of low thermally conductive, cryogenic ribbon cable drove the design process of the daughter card. Using nearly all the available space, the board was 4.25 in. x 4.00 in. and consisted of the RSI in a 256 pin grid array package, a Xilinx Spartan 3E 1200 FPGA, three MDM cable headers for the primary cabling, a 3 x 12 grid of pin headers for optional diagnostic signals, multiple sets of power rail decoupling capacitors, necessary off-chip passives for the charge channels and the ADC, and optional fixed resistors at the inputs of the high-speed and universal channels, as seen in Figure 36.

While in the dewar, a limited number of conductors could be used between the daughter card and outside world because each one created a thermal shunt from the RSI, limiting the testing temperature range. Unfortunately, the thermally resistive cryogenic conductors also had a series electrical resistance of approximately 50 Ω, so one of the three cables had to be a thermally conductive copper cable for rail current handling. The low conductor count also meant that only half of the 16 channels were accessible for testing, but at least two of each type were represented.

During over-temperature measurements, the three internal MDM cables connected

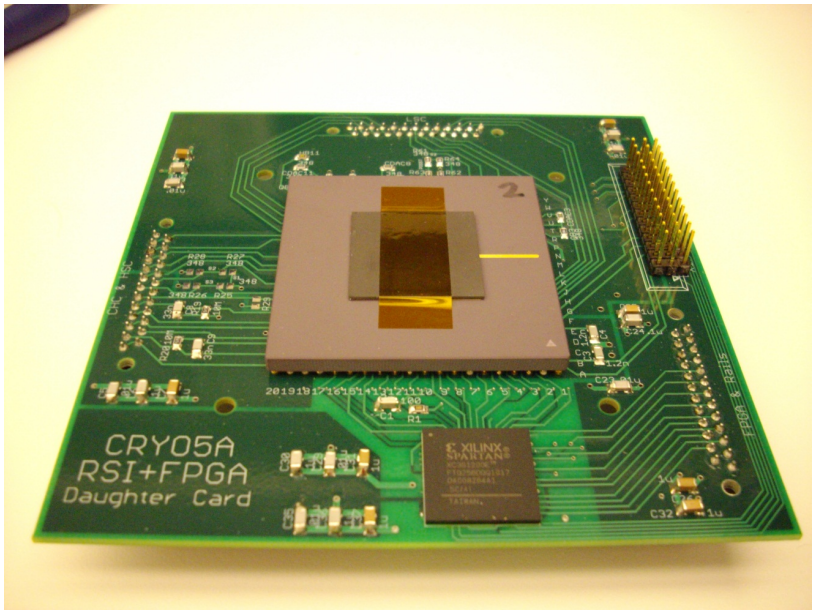


Figure 36: The RSI-with-FPGA REU in-dewar daughter card.

from the daughter card to dewar flanges and on the outside, another set of copper MDM cables connected to the motherboard. Shorting jumpers were used on the 100 mil daughter card headers to set the optional test signals to predefined DC values. When out of dewar, the three MDM cables connected directly to the motherboard, and a 26-pin ribbon cable made the diagnostic signals available for use on the motherboard.

Motherboard The motherboard contained all of the power management and interface circuitry. Five different programmable voltage regulators, each with sets of decoupling capacitors, ensured a clean voltage supply to the daughter card. Commercial ISO 11898 transceivers were used for CAN-bus communication. Pin headers were used with a USB JTAG adapter to program the FPGA. DIP switch arrays made it possible to present various Wheatstone bridge configurations and load resistances to the universal and high-speed channels. A photograph of the motherboard is shown in Figure 37.

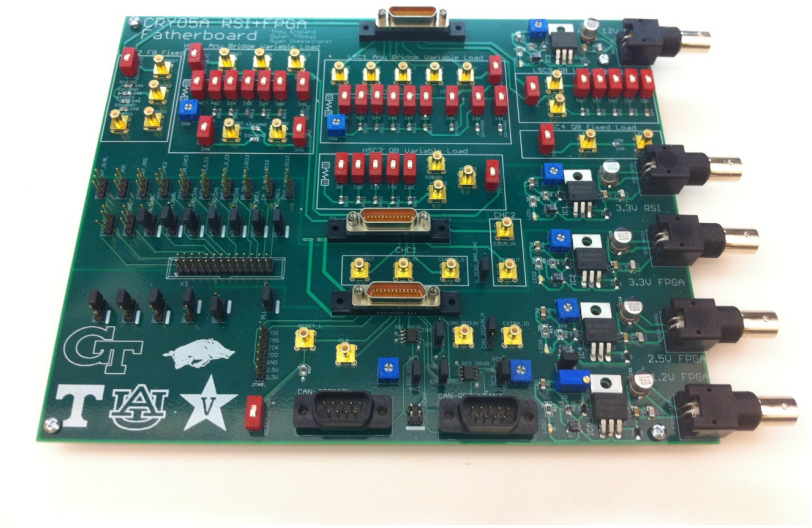


Figure 37: The RSI-with-FPGA Remote Electronics Unit motherboard.

2.4.1.3 Measurement Methods

The main measurement objective was a quantification of resolution, noise level, and system sensitivity over temperature. Resolution was defined as the amount of change of the measured element per least significant bit (LSB) of the ADC. In the case of the universal and high-speed channels the element was resistance, so the resolution can be expressed as shown in equation (1).The ADC output was saved versus five different values of the input resistor, and a linear regression fit was used to derive the resolution.

$$Resolution\left[\frac{\Omega}{LSB}\right] = \frac{\Delta R_L}{\Delta LSB} \tag{1}$$

The charge channel required special consideration. Instead of presenting an absolute charge input, a sine current source was used at the input to precisely control the change in charge over time, ΔQ. Taking advantage of the integral relationship between current and charge in (2) and analyzing the ADC output made the calculation of (3) possible.

$$\Delta Q = \int_0^{\frac{1}{2f}} Acos(2\pi ft)dt = \frac{A}{\pi f} \tag{2}$$

$$Resolution\left[\frac{C}{LSB}\right] = \frac{\Delta Q}{\Delta LSB} \tag{3}$$

Next, noise analysis information was needed. The chosen strategy was to create a standard DC output on each channel and take a transient measurement. For the universal and high-speed channels, a balanced 350 Ω Wheatstone bridge was connected to the input, ensuring the measured differential voltage was zero, and resulting in 600 mV at the output. For the charge channel a built-in ability to short internal feedback was used to produce a DC voltage on the output. The standard deviation of approximately five seconds worth of ADC samples were saved per measurement in these states and used as the noise level.

Sensitivity was then defined as the input referred noise floor of each channel. By multiplying the values of resolution and noise, the output noise level was referred back as an input source in the measured unit in RMS, as indicated below in (4) and (5).

$$Sen.\left[\Omega\right] = Noise\left[LSB\right] \times Res.\left[\frac{\Omega}{LSB}\right] \tag{4}$$

$$Sen.\left[C\right] = Noise\left[LSB\right] \times Res.\left[\frac{C}{LSB}\right] \tag{5}$$

2.4.1.4 Resolution, Noise and Sensitivity Results

The measurement methods discussed were performed for multiple gain states in each channel type during over-temperature testing from 100 K to 343 K. The resolution results for the universal channel can be seen in Figure 38. It is followed by results of the high-speed channel and charge channel in Figure 39 and Figure 40, respectively. The noise levels stay uniform for each gain state. Even in the lowest gain states, the sensitivity is better than 0.25 across the 243 K temperature range. In the higher gain

states, it improves to below 50 mΩ.

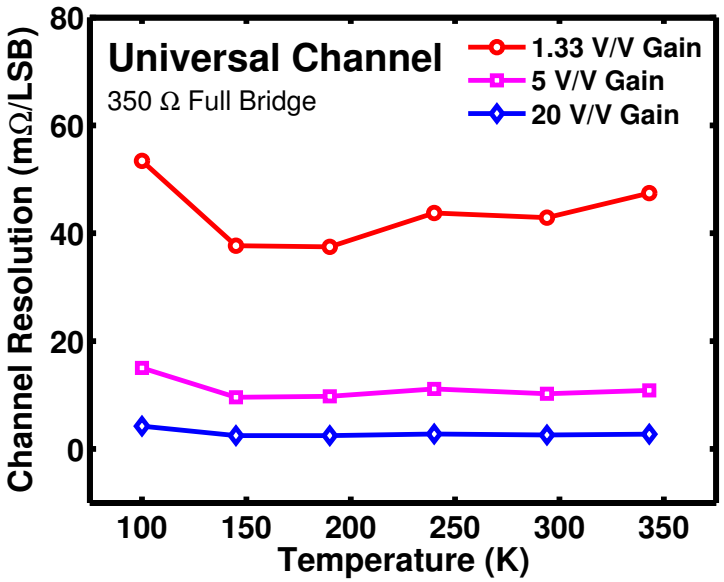


Figure 38: The universal channel resolution was consistent across the full temperature range. It was better than 60 mΩ/LSB in all cases.

Two major characteristics were evident. The gain was remarkably flat, showing little dependence on temperature over an almost 250 K temperature spread. In addition, the resolution is very tight. In the case of the universal and high-speed channels in the highest gain states, an LSB represents less than 10 mΩ. Even in the lowest gain, an LSB is less than 60 mΩ. For the charge channel in the high gain state, the resolution is approximately 0.1 pC per LSB, and it stays below 0.6 pC per LSB in the low gain state.

Along with resolution, channel noise was measured over the same temperature range. The noise data and the resulting sensitivity for the universal channel can be seen in Figure 41. It is followed by results of the high-speed channel and charge channel in Figure 42 and Figure 43, respectively. Except for occasionally falling off at the top and bottom ends of the temperature range, the noise levels stayed uniform for each gain state and fell far below the full scale range of 4096 LSBs. The universal channel had the best noise performance, staying below 6 LSBs over the entire temperature

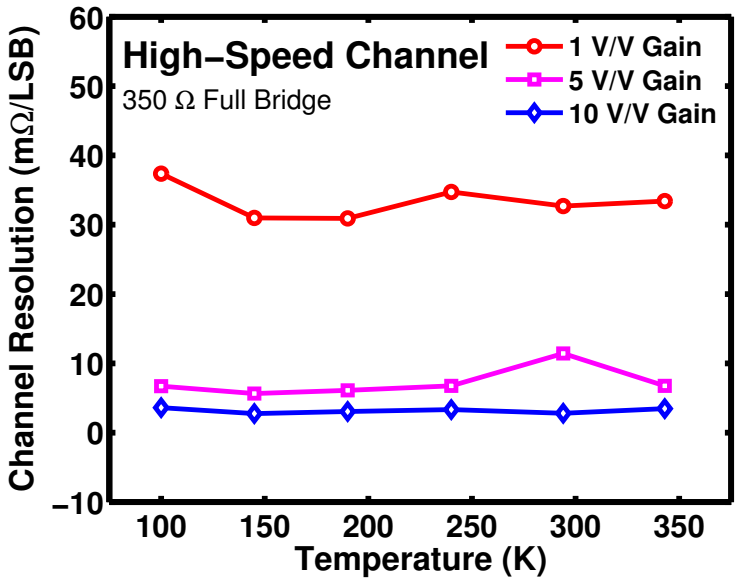


Figure 39: The high-speed channel resolution was consistent across the full temperature range. It was better than 40 mΩ/LSB in all cases.

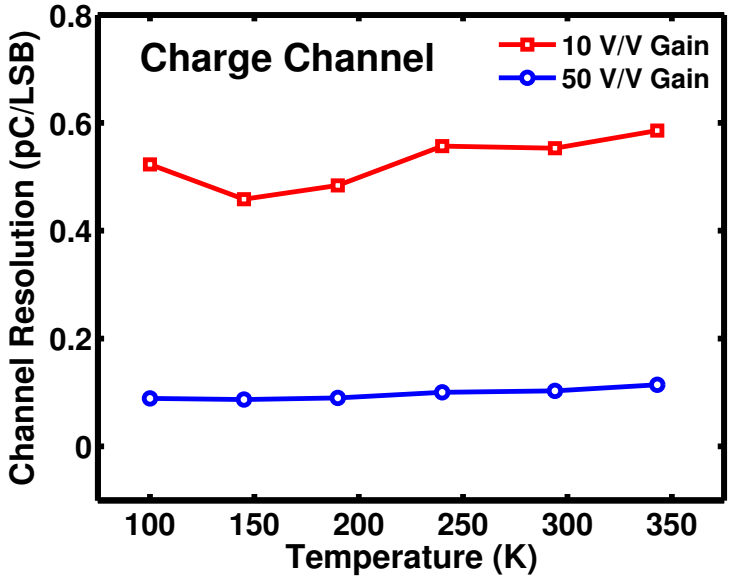


Figure 40: The charge channel resolution was consistent across the full temperature range. It was better than 0.6 pC/LSB in all cases.

range. The high-speed and charge channels were consistently below 30 LSBs. A 6 and 30 LSB noise floor would result in a single, full-scale tone signal to noise ratio (SNR) of 47 and 33 dB, respectively.

Sensitivity was calculated from the product of the noise and resolution. It represents the input-referred noise source and can be interpreted as the measurement noise floor of the channel. Even in the lowest gain states, it stays below 0.25 Ω across the 243 K temperature range. In the higher gain states, it improves to below 50 mΩ, meaning that this REU implementation can reliably detect any change above 50 mΩ in resistance at any temperature between 100 and 343 K. For the charge channel, sensitivity stays better than 15 pC and 5 pC in the low and high gain states, respectively.

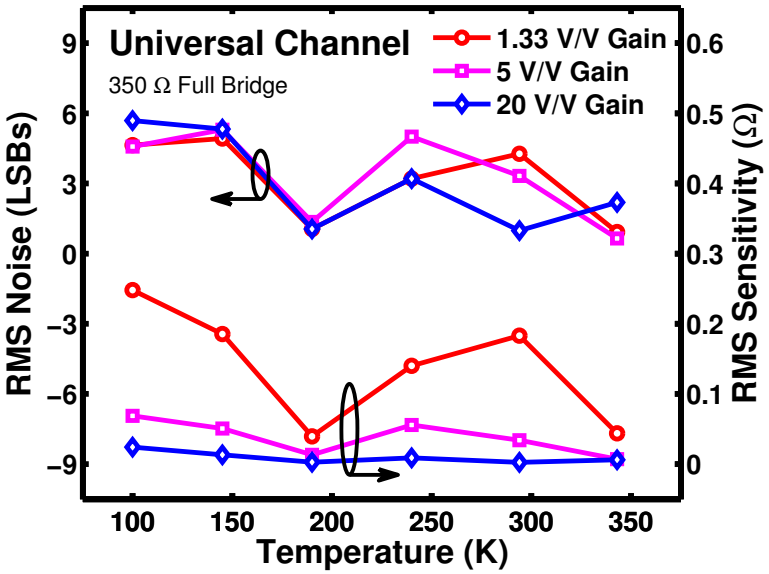


Figure 41: The universal channel noise was the lowest of all three channels and remained below 6 LSBs RMS across the full temperature range. The sensitivity was better than 300 mΩ RMS in all cases and better than 25 mΩ RMS in the highest gain state.

2.4.2 Radiation Experiments

The RSI was subjected to TID exposure at Vanderbilt University and SEE testing over temperature at the Cyclotron Institute at Texas A&M University. A TID exposure of

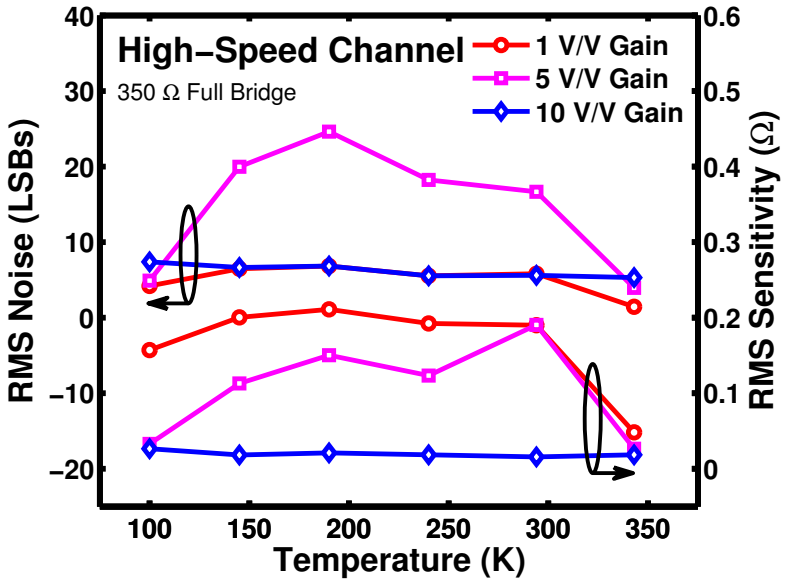


Figure 42: The high-speed channel noise was below 10 LSBs RMS across the full temperature range for the highest and lowest gain states. The sensitivity was better than 300 mΩ RMS in all cases and better than 50 mΩ RMS in the highest gain state.

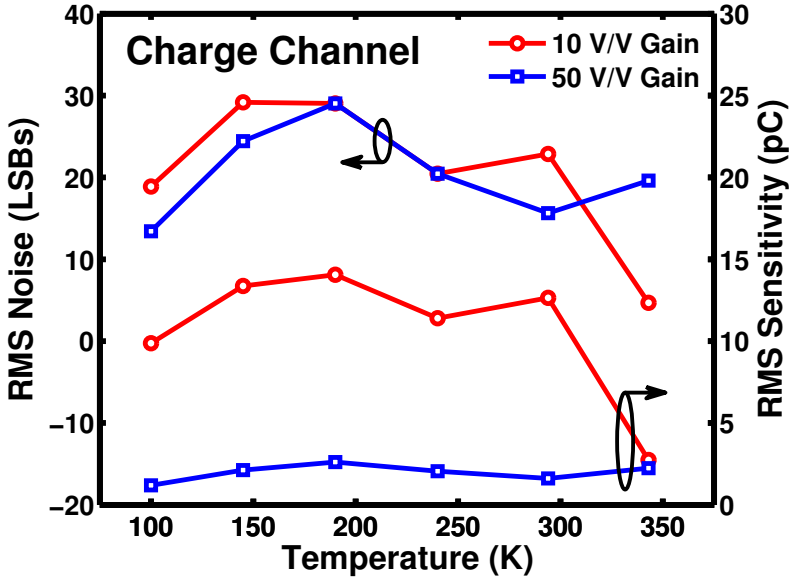


Figure 43: The charge channel noise was below 30 LSBs RMS across the full temperature range. The sensitivity was better than 15 pC RMS in all cases and better than 5 pC RMS in the highest gain state.

100 krad revealed no observable degradation in the RSI operation. Noise values and supply currents were not noticeably altered between pre-exposure and post-exposure.

2.4.2.1 Over-temperature SET Analog Noise Quantization

To quantify the effects of single-event transients (SETs) on the RSI, the same noise measurements from the original over-temperature characterization were performed while the RSI was being subjected to broad beam irradiation using a variety of heavy ions and exposure temperatures. The test setup utilized the radiation dewar described previously. The RSI was exposed from 85 K to 293 K. The heavy ions used were $_{20}$Ne, $_{40}$Ar, $_{84}$Kr, and $_{129}$Xe. After factoring in the energy losses in air and through the Aramica windows using TRIM [37], the resulting surface linear energy transfer (LET) values were 2.5, 8.3, 29, and 57 MeV·cm^2/mg, respectively. We observed an overall trend of higher noise level with increasing LET, as shown in Figure 44. The effect was observable at lower LETs, but became more significant with LETs above 20 MeV·cm^2/mg.

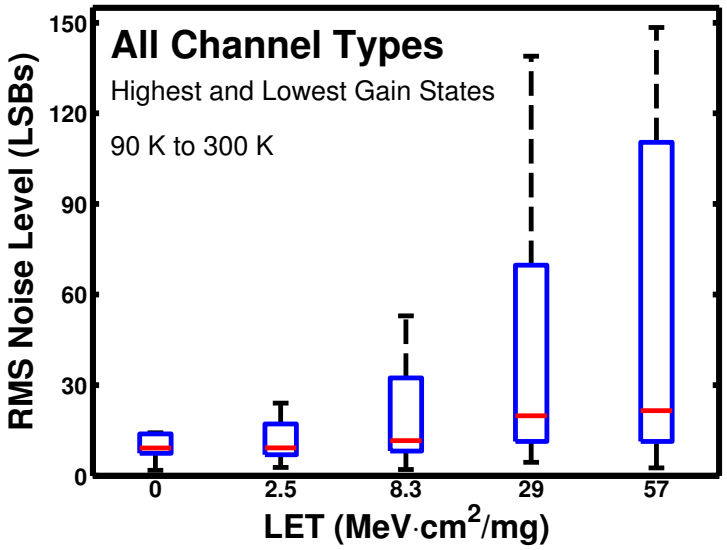


Figure 44: A box and whisker plot showing noise levels across all temperatures and channel types for the higest and lowest gain states.

For single-event latchup testing, the RSI was exposed at 125 °C to a fluence of

1.0 x 107 ions/cm^2 of 129Xe ions at three different angles of incidence: 0°, 30° and 45° (LET = 47.3 MeV·cm^2/mg at 0°). Currents were monitored in real-time with an Agilent 6624A four-channel power supply set to detect any rise above critical limits. Throughout the test, no latchup was observed; supply currents stayed within safe tolerance, and throughout all radiation experiments (TID, SET Noise, and SEL) no catastrophic failures ever occurred, indicating that the RSI is SEL immune, as intended.

2.4.3 Summary

This work presented the over-temperature and radiation testing of a complex, 16-channel, extreme environment capable, SiGe REU containing the RSI ASIC that can serve a wide variety of space-relevant needs as designed. These include future missions to the Moon and Mars, with the additional potential to operate in other hostile environments, including lunar craters and orbits of the Jovian moons. The performance of the chip has been verified over an almost 250 K temperature range and against 100 krad TID radiation exposure. It was shown to be latchup immune and have the ability to operate across temperature in a high-flux heavy-ion environment. Furthermore, it retained the key functionality of the RHN while exhibiting improvements of an order of magnitude in volume, weight, and power over the RHN as shown in Table 4.

Table 4: Specification Improvement of REU over RHN

Specification	**RHN**	**REU**	**Improvement**
Volume	101 in^3	10.1 in^3	10x
Weight	24 lbs.	1 lbs.	10x
Power	17 W	1.5 W	10x
Temperature Range	−55 to +120 °C	−180 to +120 °C	125 °C
TID Tolerance	Vulnerable	100 krad	Hardened

This work successfully demonstrated that a commercially available SiGe BiCMOS technology platform could be used to support extreme environment electronics needs

without costly, centralized "warm-boxes" and "electronics vaults," opening the possibility of dramatic improvements in spacecraft size, weight, and power.

CHAPTER III

LOW-FREQUENCY NOISE IN SIGE BICMOS PLATFORMS AT CRYOGENIC TEMPERATURES

In 2006 the scientists of Fermi National Accelerator Laboratory (FNAL) and Brookhaven National Laboratory (BNL) began the US Long Baseline Neutrino Experiment Study. It sought to identify the best method to study neutrino mixing that could be responsible for the phenomenon of neutrino oscillations. One of the experimental methods discussed was the use of a giant liquid-argon time-projection chamber (TPC) [38]. The utilization of a time-projection chamber is a common method to detect particle collisions. When particles interact with the environment, they tend to generate free electrons. The TPC collects those electrons with successive nets of parallel conductors. Voltages placed across adjacent conductors results in electric fields that help to collect the free electrons. Combining the charge collection data for each net, scientists can create a three-dimensional mapping of the particle path. The study suggested the use of a larger than normal TPC to increase measurement fidelity. The proposed giant liquid-argon TPCs were between 20 and 100 kton [39].

At the proposed sizes, it was impractical to have the detection electronics outside the chamber as the conductors would have to be too long and the measurement would have been degraded. In an effort to preserve the sensitivity of the measurement, the project proposed moving the electronics inside the liquid argon environment at about 87 K [7]. These in-environment electronics promised major benefits by having the critical signal processing adjacent to the conductors rather than far away, avoiding the added noise. However, for this approach to be viable, a technology platform was needed that could meet rigorous specifications while being wide-temperature tolerant.

As mentioned in the previous chapter, SiGe BiCMOS technology has been shown to be a practical choice for wide-temperature applications. The combination of SiGe HBTs with standard Si CMOS provides high-performance analog options while maintaining compatibility with standard silicon manufacturing, and the wide-temperature performance of the SiGe HBT is well established. As the SiGe HBT approaches cryogenic temperatures, the most important device metrics for circuit design improve: current gain, transconductance, f_T, f_{MAX}, and broadband noise. Moreover, SiGe HBTs have been shown to be robust not only at 77 K but down to 300 mK [19–22].

In further effort to reduce the noise, the bandwidth of the circuitry was limited. When reducing bandwidth, it is common to keep cut-off frequencies down to the MHz or kHz range. At these lower frequencies, it is not thermal but low-frequency, also called flicker or "one over f" (1/f), noise that is dominant.

Flicker noise in MOSFETs and bipolar transistors has been a topic of study for decades [7, 40–49]. Despite this nearly half-century of research, the physical reasons for 1/f noise in Si MOSFETs is still not conclusively proven [49]. The community is split between variations in either carrier mobility or carrier number. Recent studies have suggested both are important [50]. Because of the contention, the temperature dependence of 1/f noise cannot be reliably predicted across CMOS technologies. It has been shown that in some processes, the amount of 1/f noise does not appreciably change at cryogenic temperatures [7,48]. However, in one technology, the pMOSFET noise remains constant down to cryogenic temperatures, but the nMOSFET 1/f noise level varies widely [42]. Clearly, testing is required for prediction of MOSFET noise levels at cryogenic temperatures.

One aspect of 1/f noise that is well understood, however, is that at room temperature, the vertical transport in bipolar transistors, including the SiGe HBT, tends to provide better flicker noise performance over the horizontal, surface carrier transport in Si MOSFETs [47]. Additionally, the research of low-frequency noise in bipolar

transistors has led to the understanding that the input-referred noise is strongly dependent on the base terminal current [41]. Unfortunately, like Si MOSFETs, the dependence of 1/f noise on temperature in these transistors is not well understood [47]. One experiment showed very little noise change versus temperature at constant base current in similarly fabricated Si BJTs and SiGe HBTs [41]. On the other hand, Bruce et al. suggested that the temperature dependence is not appreciable because 1/f noise is based on collector current, a departure from the classical base current dependence [46]. Much like MOSFETs, prediction of SiGe HBT flicker noise levels at cryogenic temperatures is still based heavily on experimental data and empirical relationships.

In most circuits, the last pieces of the low-frequency noise puzzle are the resistors. In wide-temperature designs, the p-type polysilicon resistors are often the best choice because of their low temperature coefficient [26]. Fortunately, flicker noise in these resistors has attracted some attention in the community. Most studies have derived empirical fits to experimental data [51–54], but some investigation into physical mechanisms has been pursued [12]. It is largely agreed that the noise has a bias dependence based on the terminal voltages and/or currents. Additionally, two papers have looked into the over-temperature behavior of polysilicon resistors, though not down to cryogenic temperatures [54, 55]. Both experiments showed a weak dependence on temperature, but they conflicted on the sign of that dependence. To first order, designers can expect the resistor 1/f noise to be constant across temperature, but exact solutions still require measurements.

This work studied the cryogenic capabilities, especially low-frequency noise, of IBMs 7WL process, a second-generation 0.18 μm BiCMOS technology, and leveraged that knowledge for low-noise voltage reference design.

3.1 Over-temperature Characteristics

IBM 7WL includes a great deal of active device options, including 0.18 μm minimum gate-length nMOS and pMOS transistors, NPN SiGe HBTs of various performance levels, and vertical Si PNP BJTs. To begin to understand cryogenic circuit design in this process, over-temperature device measurements were under-taken. The SiGe HBT Gummel characteristics with current gain inset are shown Figure 45. The increase in current gain at 90 K was of interest as most devices utilized in circuits will be current biased, and improvements would help to keep I_B and, consequently, low-frequency noise low. The Si PNP current gain was important for the opposite reason. Its Gummel and current gain characteristics are shown in Figure 46. As expected the gain fell near cryogenic temperatures, which could have potentially caused increases in low-frequency noise at given collector current biases. Near the expected current bias of approximately 1 $\mu A/\mu m^2$, the degradation was about 30 %.

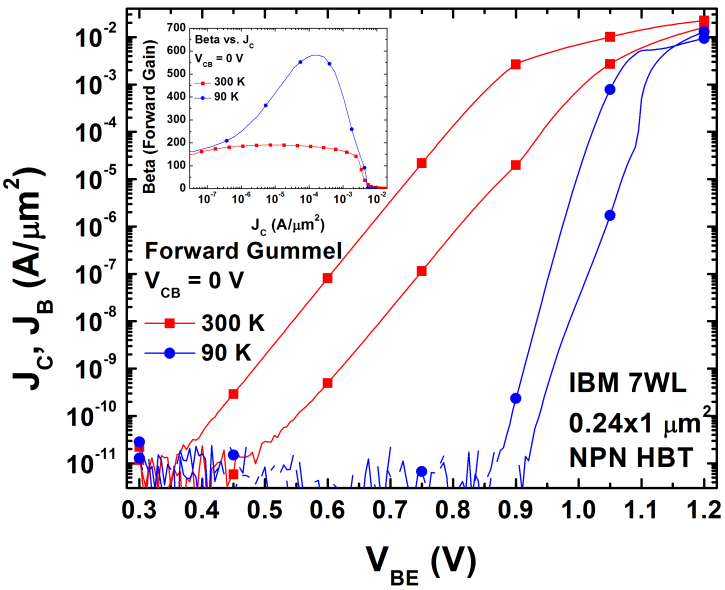


Figure 45: NPN over-temperature characteristics. The SiGe NPN current gain increases near 90 K, helping to keep low-frequency noise at a minimum.

The MOSFET transfer characteristics are shown in Figure 47. As expected, the

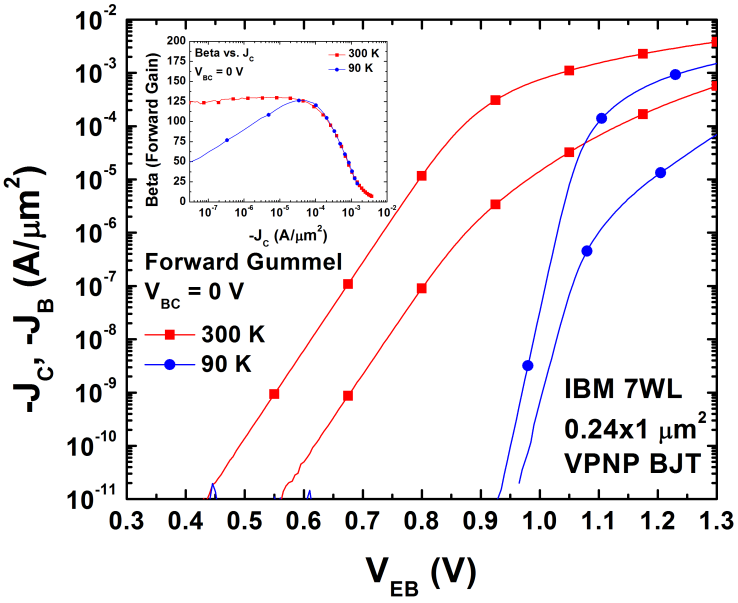


Figure 46: PNP over-temperature characteristics. The Si PNP current gain decreases near 90 K, which could cause an increase in low-frequency noise.

magnitude of I_{DSMAX} for both transistors increased indicative of the rise in mobility. The enhanced mobility often leads to the generation of more hot carriers and a worsening of reliability at cryogenic temperatures. Fortunately, the increase in transconductance reduces the input-referred low-frequency noise.

3.2 Low-frequency Noise Characteristics

Given the high priority placed on noise performance, the low-frequency noise of the transistors was measured at both room and cryogenic temperatures. The SiGe HBTs input-referred base-current noise at room temperatures showed an approximate I_B^2 bias dependence, as has been shown in the past [41]. At cryogenic temperatures, the dependence shifted to about I_B^1. The spot noise at 10 Hz is shown in Figure 48. At the anticipated bias points ($I_B < 10$ nA), the cryogenic noise was higher than the room temperature values. The input referred base current noise of the vertical PNP was slightly higher but showed the same I_B^2 dependence as the SiGe HBT. Unlike the

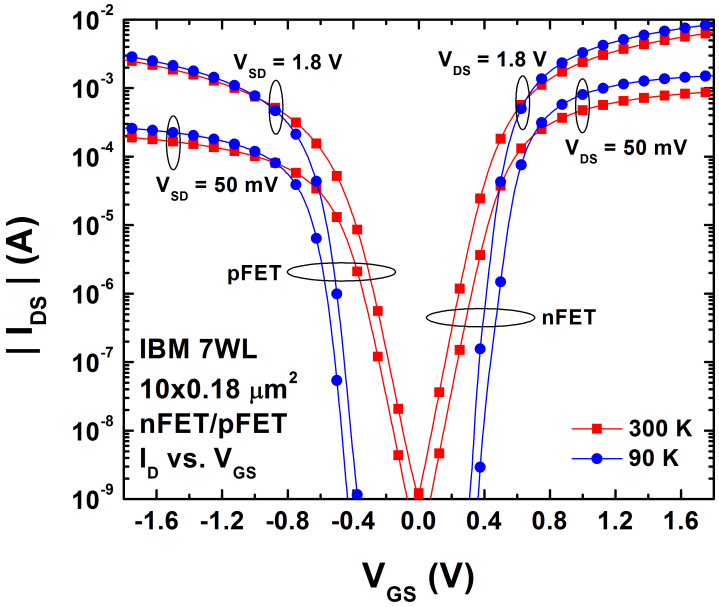


Figure 47: Both nFET and pFET over-temperature transfer characteristics. The increase in mobility near cryogenic temperatures can help to lower input-referred noise.

SiGe HBT, the I_B dependence did not drastically change at cryogenic temperatures, and the noise degraded over entire range of bias measurements.

FET noise testing was focused in moderate and strong inversion. At room temperature, the nFET input-referred gate voltage noise levels were largely independent of bias, but the pFET noise had some dependence as shown in Figure 49. This was similar to the behavior observed in another 0.18 μm technology [50]. At cryogenic temperatures both the nFET and pFET exhibited a very light bias dependence ($I_D^{0.2}$) with large variation across bias. Variations on this order have been observed in submicron technologies before [49]. Overall, the noise voltage fell over the entire bias range for both devices at 90 K. The pFET noise was higher at room temperature, but fell to be nearly equal to the nFET at the lower temperature.

Comparisons of the bipolar and FET noise had to be undertaken to understand the trade-offs between the two transistor types. Given the differences in basic device physics and noise sources, any comparison was imperfect. In general, the 1/f noise in

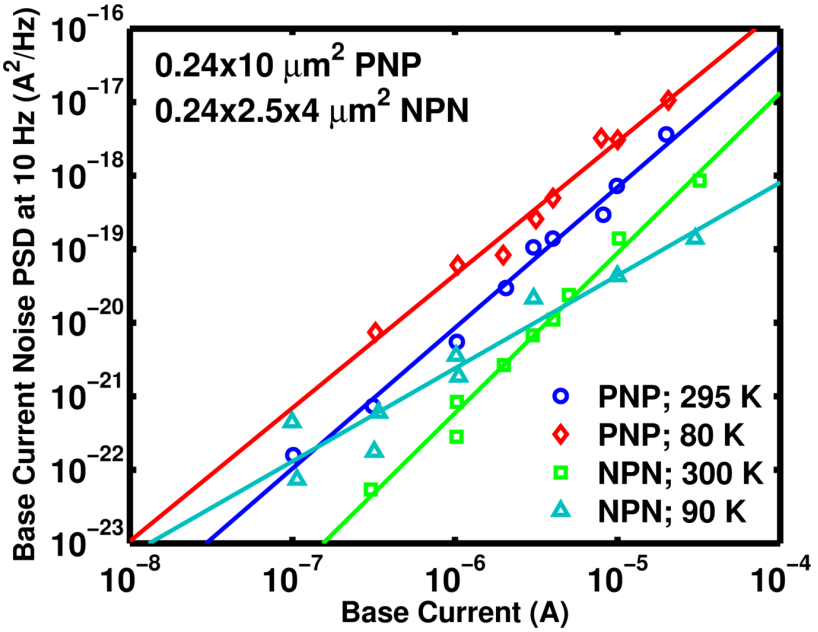


Figure 48: Base current noise PSD in the SiGe NPN and Si PNP near 300 K and 90 K at 10 Hz over bias. The bias dependence of the NPN noise changed, but the PNP bias dependence stayed the same.

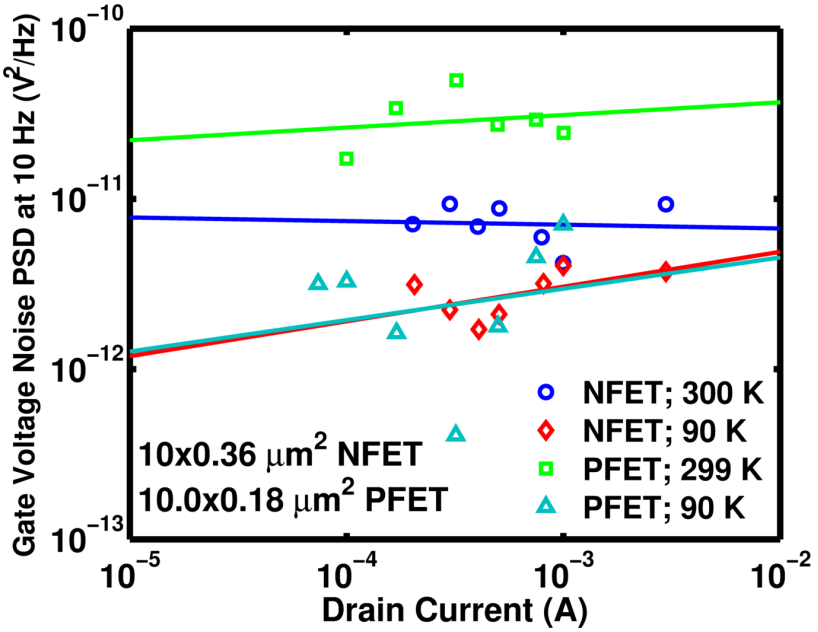


Figure 49: Gate voltage noise PSD in the nFET and pFET at 300 K and 90 K at 10 Hz over bias. At room temperature the nFET showed no bias depedence, but the pFET showed weak bias dependence. At 90 K both developed a weak $I_D^{0.2}$ dependence.

MOSFETs is known to be best modeled as a current noise source between the drain and source terminals, but in bipolar transistors the noise source is best modeled as a current source between the base and emitter terminals. Consequently, the output noise of bipolar transistors can be reduced by a low input resistance at the base. In this case, the comparison is of input-referred noise voltage, which favors the FETs as it assumes an impossible condition, an infinitely high-impedance voltage noise source for the bipolar transistors. In the n-type comparison, the NPN showed slightly better 1/f noise performance than the nFET at both room and cryogenic temperatures, as shown in Figure 50. The SiGe NPN input referred noise voltage is slightly lower than the nFET at similar current bias at room temperature, and improves more than the nFET does at 90 K.

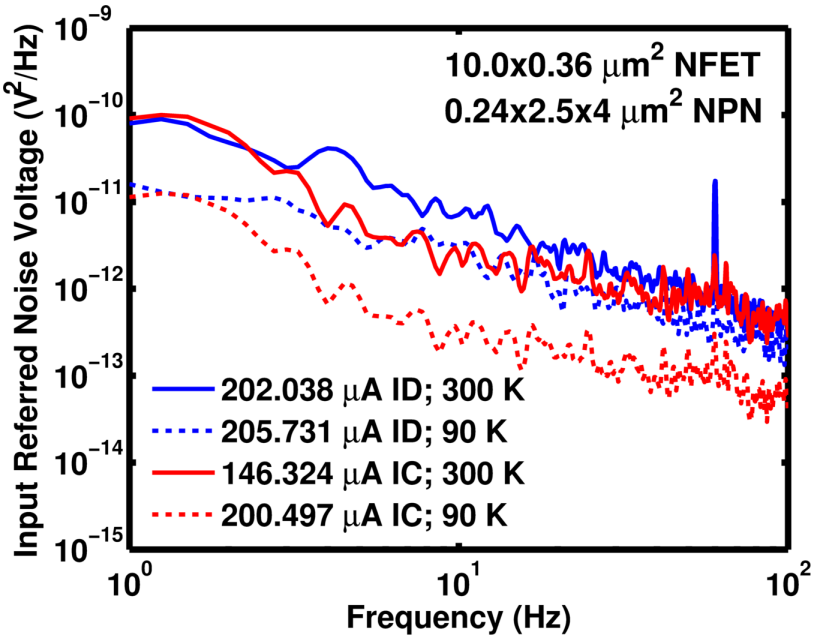


Figure 50: Measurements of input referred noise voltage of both an nFET and SiGe NPN HBT at room and cryogenic temperatures. The NPN had slightly better noise performance at both temperature points.

The results of the p-type comparison were less clear. At room temperatures, the Si PNP had better 1/f noise performance as shown in Figure 51. However, as the devices were taken down to cryogenic temperatures, the benefits of the bipolar

transistor became less clear. The drop in the Si PNP current gain compounded the noise performance loss already shown in Figure 48. At a given collector/drain current, the Si PNP noise degraded to levels worse than the pFET. Clearly, the inconsistency created complications for circuit design at cryogenic temperatures, so two variants of each circuit topology were designed: one using pFETs and one utilizing PNPs.

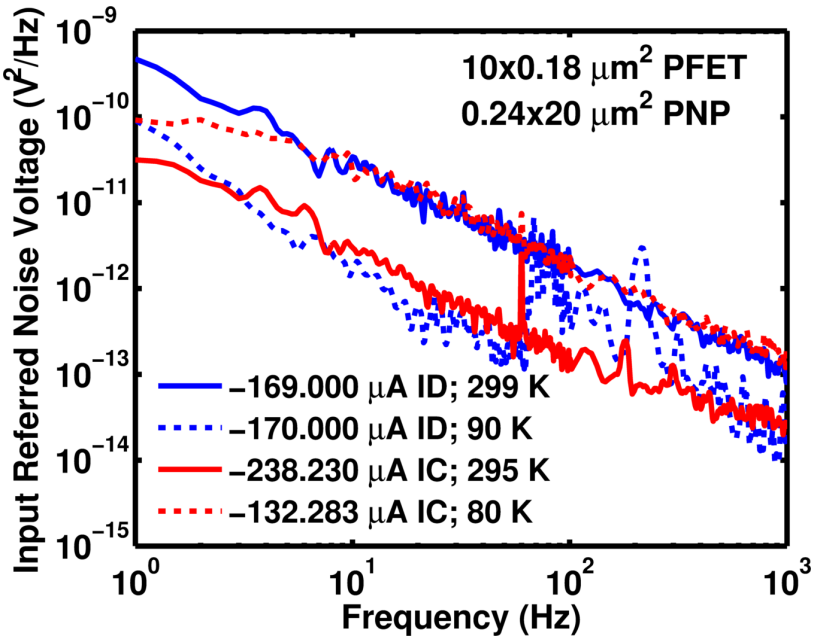


Figure 51: Measurements of input referred noise voltage of both a pFET and a Si PNP at room and cryogenic temperatures. The PNP outperforms the pFET at room temperature but becomes worse at cryogenic temperatures.

The final low-frequency-noise tests were of the polysilicon resistors selected for use in the circuit designs. The noise followed an I_R^2 dependence at both 290 K and 90 K, and the overall level fell slightly at 90 K, as shown in Figure 52. The results agreed with the temperature dependence derived in [55].

3.3 Voltage References

Two topologies of voltage references were designed as a part of this work [56]. They both used the PTAT current source found in [57] and introduced in [58] for high power-supply rejection at low rail voltages. For each topology, two versions were

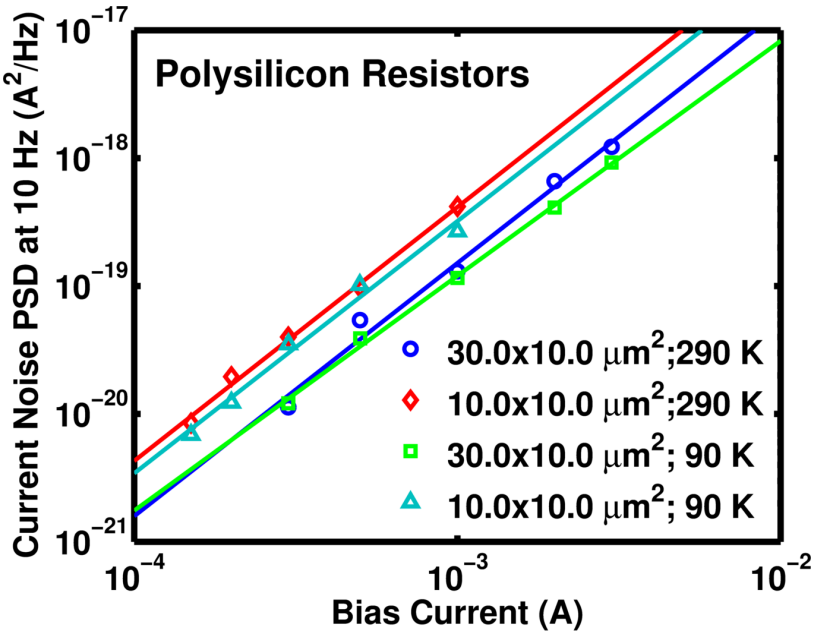


Figure 52: Resistor current noise PSD at 10 Hz at 290 K and 90 K. The resistor noise was nearly constant over the temperature range and maintained an I_R^2 dependence across the entire measurement range.

designed: one using the vertical Si PNP BJTs and one using PFETs.

The first topology used a basic diode-connected SiGe NPN HBT and resistor for the CTAT and PTAT voltage generation respectively, as shown in Figure 53. The transimpedance gain from the PTAT current to the output voltage could be written as shown in (6).

$$Z_{ptat1} = \frac{v_o}{i_{ptat}} = R_2 + \frac{1}{g_{mQ4}} \tag{6}$$

The second topology utilized a more complex cell based on the original Widlar design [59]. It is shown in Figure 54. The cell used negative feedback to establish the CTAT operating point and compensate for the noise in the PTAT current reference [56]. The transimpedance gain from the PTAT current to the output voltage could be written as shown in (7).

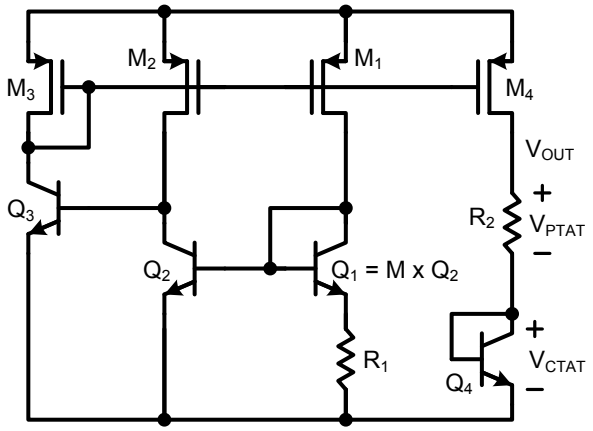


Figure 53: A schematic of the simple BGR topology that suffers from noise from the PTAT current source.

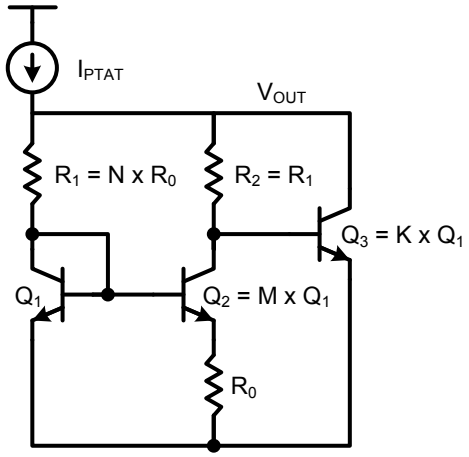


Figure 54: A schematic of the Widlar cell used in the second BGR topology that reduces the influence of the noise from the PTAT current source.

$$Z_{ptat2} = \frac{v_o}{i_{ptat}} = \left\{ \frac{1+\beta_3}{R_2 + r_{\pi 3}} + \frac{g_{m1}}{1 + g_{m1} R_1} \left[1 - \frac{1}{1 + \ln M} \left(\frac{R_2 \beta_3 - r_{\pi 3}}{R_2 + r_{\pi 3}} \right) \right] \right\}^{-1} \quad (7)$$

The calculated values of the transimpedance gains from the PTAT current source to the output voltage are shown in Table 5. At both 300 K and 90 K, the Widlar topology transimpedance gain is nearly and order of magnitude lower than the basic topology.

Table 5: Comparison of the gain from the PTAT current to the output in both BGR topologies.

Temperature	Basic CTAT	Widlar CTAT
300 K	2400 Ω	381 Ω
90 K	1885 Ω	240 Ω

The first topology suffered because of the larger dependence on the noise of the PTAT current source. The output noise followed the same trends as the pMOS and PNP followed in device testing. As shown in Fig. 55, at room temperature the PNP version had superior noise performance, but at cryogenic temperature, the noise had increased such that the pFET version performed better. The effect of adding the feedback in the Widlar topology was evident in the measurement results. As can be seen in Figure 56, the noise over temperature was less dependent on the devices used in the PTAT current generator, meeting or exceeding the best performance levels of the simple BGR at both temperatures.

3.4 Summary

This work studied the cryogenic capabilities, especially low-frequency noise, of IBMs 7WL process, a second-generation 0.18 μm BiCMOS technology, and leveraged that knowledge for low-noise voltage reference design. It was shown that the use of negative feedback techniques alongside SiGe NPNs could mitigate the transistor noise from

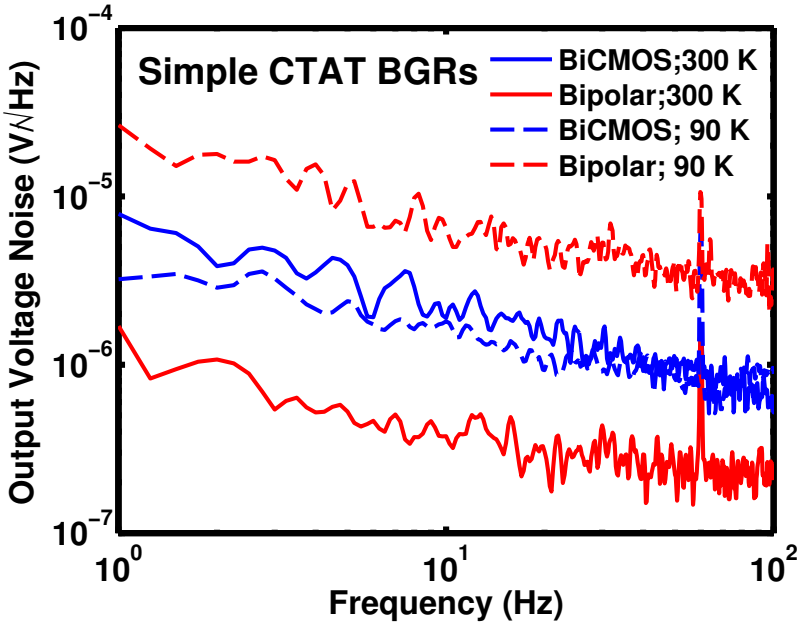


Figure 55: Output noise of the simple CTAT BGR. This BGR topology suffers from a direct noise dependence on the PTAT current source (pFETs or PNPs). The bipolar version has better noise performance at room temperature, but the BiCMOS is superior near cryogenic temperatures.

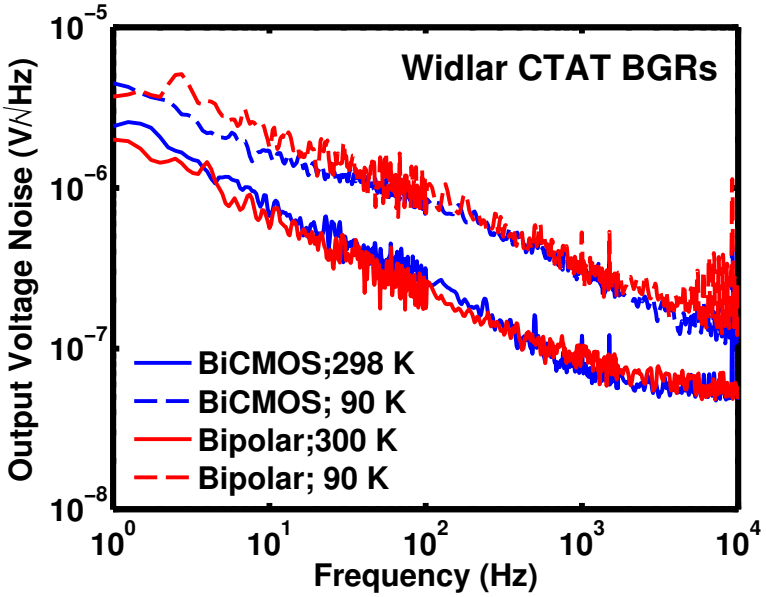


Figure 56: Measurements of output noise voltage of both variants of the second BGR topology. The output varies less over temperature and versus the types of devices used in the PTAT current source.

the pFETs and Si PNPs and lead to an overall reduction in output noise of voltage references at both 300 K and 90 K.

CHAPTER IV

RADIATION TOLERANCE OF ADVANCED SOI CMOS TECHNOLOGIES

SOI technologies have enjoyed a niche market in the aerospace sector for decades because they generally have better SEE radiation response compared to bulk processes. Gasiot et al. found the SEE robustness of SOI to be superior to bulk, especially in body-source-connected devices in SRAM cells [60]. At the same time, Gadlage et al. showed that SET widths in a 180 nm fully depleted SOI devices were both temperature invariant and an order of magnitude shorter than a 130 nm bulk devices [61]. The SEE tolerance of SOI technologies is attractive, but their hardness against TID is questionable. SOI tolerance to TID effects is usually lower compared to bulk processes due to the buried oxide, but with some processing techniques, it can be equal [62].

Forecasts for the future of the single event tolerance of all Si CMOS devices, both bulk and SOI, predict increased sensitivity with scaling [63]. Dodd et al. used three-dimensional mixed-level device and circuit simulations to derive threshold levels for single-event transients and upsets in both bulk and SOI technologies, showing a worsening trend with scaling [64]. Worse still, the parasitic bipolar amplification in floating-body SOI devices can degrade the SEE hardness of SOI technology down to bulk device levels [65]. For SOI to continue to be a major factor in extreme environment electronics, more investigation is needed in the overall SEE sensitivity and single-event transient behavior of highly scaled generations of these technologies.

One methodology for SEEs analysis is laser-induced carrier creation using two-photon absorption (TPA). Implemented in 2002 by McMorrow et al. at the Naval Research

Laboratory, the TPA methodology uses sub-band gap lasers to generate carriers in semiconductor materials [66]. It creates carrier mimicking tracks formed by heavy-ion irradiation, and correlation of the two is a continuous topic of research [67, 68]. The facility allows for three-dimensional analysis using a fine-resolution mechanical stage [69]. All of these features make TPA an excellent method for studying single-event effects in SOI technologies.// To bring further understanding to the projection of scaling-induced SET sensitivity in SOI CMOS technology, this work uses charge deposition by TPA to present the first investigation of the physical mechanisms underlying the single-event transient response of cascode amplifier cores in a 45 nm RF-CMOS/SOI technology, includes a study of transient propagation in 32 nm differential pairs, provides the first experimental comparison of SET between 45 nm and 32 nm RF-CMOS/SOI devices, and presents implications for circuit design in both technologies. It leverages a number of different device types and is supported by calibrated 45 nm cascode TCAD simulations.

4.1 Experimental Details

The 45 nm (IBM 12SOI) cascode structures consisted of two 20-finger "analog" threshold voltage nMOSFETs. Each MOSFET was either 1.0x0.040 μm^2 per finger with a floating body, or 1.0x0.056 μm^2 per finger with notched-T body contacts. The three cascade cores varied in the combination of the two types of FET utilized (Figure 57). The drawn layout parameters of each cascode transistor are summarized in Table 6. The total drain area of the body-contacted devices was approximately twice that of the floating-body variants due to the doubled gate pitch, accommodating the contacts.

The 32 nm (IBM 32SOI) differential pair structures consisted of four transistors and two resistors: two four-finger pMOSFETs as the differential pair, two current mirroring pMOSFETs as the current input and tail source, and two resistors as the

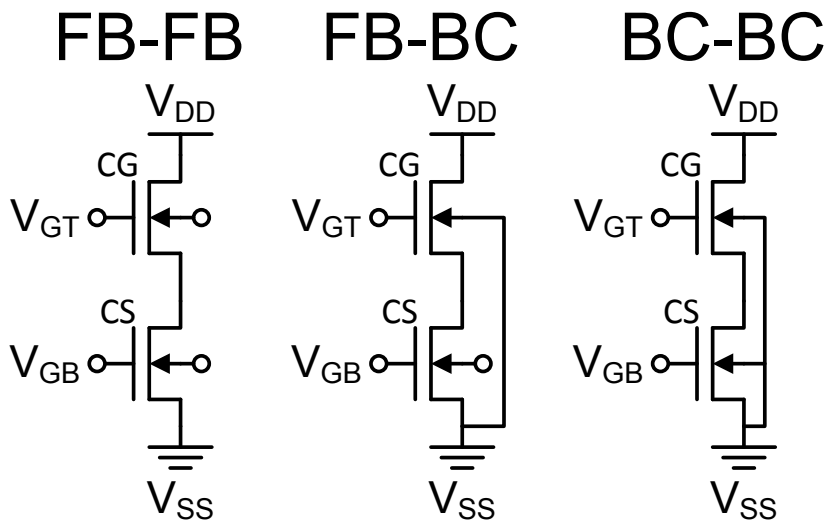


Figure 57: Schematics of the three cascode amplifier cores for comparison. Each cascode consisted of a common-source (CS) and common-gate (CG) amplifier. If body contacts were present, they were connected to VSS.

Table 6: 45 nm multi-finger device drawn layout parameters.

Body Contact	**Active Width (μm)**	**Gate Length (μm)**	**Gate Pitch (μm)**	**Total Drain Area (μm^2)**
None/Floating	1.007	0.040	0.190	1.51
Notched-T	1.000	0.056	0.380	3.12

loads (Figure 58). All transistors were "analog" threshold voltage. Each differential pair pMOSFET was 1.3x0.056 μm^2 per finger and notched-T body contacted to the source terminal. Both current mirror transistors were 1.3x0.230 μm^2 per finger notched-T-body-contacted pMOSFETs with 12 fingers. The differential pair was loaded with 2 kΩ on-chip resistors.

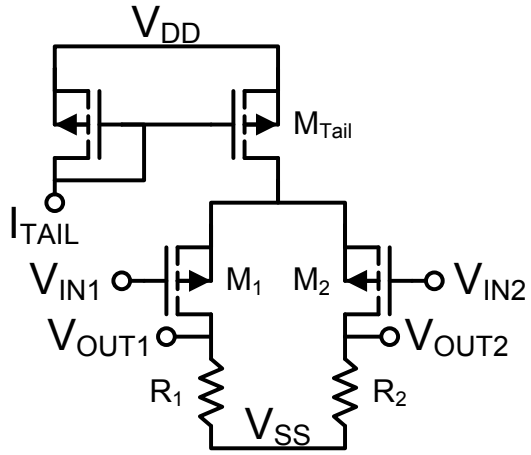


Figure 58: A schematic of the differential pair structure used in the TPA experiment. It consisted of four body-contacted pMOS transistors and two 2 kΩ resistors.

Additional samples studied were multi-finger 45 nm devices of the same geometry as those in the cascode and three floating-body, single-finger devices from the 45 nm (IBM 12SOI) technology and 32 nm (IBM 32SOI) technology. Finally, a calibrated, 45 nm cascode TCAD model was utilized to simulate ion strikes in similar cascode variants. The model has most recently been proven useful in understanding electrical stress experiments [14].

Laser-induced transients were measured at the Naval Research Laboratory in Washington, DC, using charge deposition by through-wafer two-photon absorption capable of supplying a 1.0-μm FWHM diameter charge distribution profile [66]. This system enabled 3-D position-dependent, time-resolved measurements of single event transients. It induced device-level current transients by injecting carriers using TPA from a sub-bandgap pulsed laser. The TPA system was configured to produce optical

pulses at 1260 nm, a repetition rate of 1 kHz, and a pulse width of approximately 150 fs. The xyz translation platform had a position resolution of 0.1 μm. All data were collected in a rectangular xy grid at a fixed "z." Upon inserting each DUT, the "z" position was optimized to place the sensitive volume at the peak focus of the laser beam.

Transients were recorded using high-bandwidth measurement equipment, including a Tektronix DPO71254 12.5 GHz, 50 GS/s, real-time oscilloscope. DC biasing was accomplished using bias-tees to separate the DC levels from the fast transients. To improve measurement accuracy, a number of sequential transients were captured at one time. In those cases, error bars are present in the figures, representing the standard deviation within those sets of transient captures. An equivalent schematic of the measurement setup for the cascode structures is show in Figure 59.

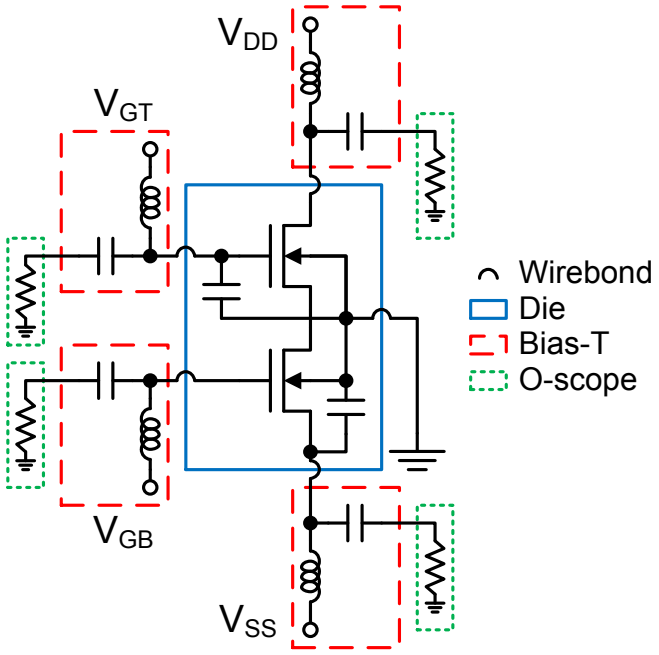


Figure 59: Schematic of the cascode experimental setup including bias tees and oscilloscope inputs. On-chip decoupling capacitors were included for high frequency measurements from previous work [14].

4.2 Results and Discussion

4.2.1 Cascode Cores Experiment

The cascode structures were first analyzed with respect to overall SET sensitivity. 2-D raster scans (Figure 60) showed immediately that for all three body contacting schemes, charge generation in the common-source (CS) amplifier device resulted in larger amplitude transients than charge generation in the common-gate (CG) amplifier device. The dissimilarity, in a small-signal sense, was due to the relative differences in impedance seen by each of the devices looking into the other. The CS amplifier looked into the source terminal of the CG device, a relatively low-impedance terminal, which conducted current variation with small changes in terminal voltage. On the other hand, the CG device looked into the drain of the CS transistor, a relatively high-impedance terminal. Current changes in the CS device drain required relatively large voltage variation. A physics-based discussion of these observations proceeds in the TCAD simulation section.

The next observation came from comparing the impact of the three body contacting schemes on SET response. The presence of body contacts consistently reduced the peak transient despite the body-contacted devices having larger active areas, as is illustrated in Figure 61. The difference was attributed to charge amplification through the parasitic bipolar present in SOI MOSFETs [65].

The bipolar amplification of generated charge takes place during strikes in voltage-biased SOI FETs where generated electrons are naturally swept out of the drain by the electric fields present inside the device. The activity of the holes depends on the presence of body contacts. In body-contacted devices, holes can promptly leave the devices through nearby body contacts and avoid charge amplification. However, during strikes in floating-body devices, holes can accumulate in the body region, raising the potential to the point that appreciable diffusion current takes place across the body-source junction. The uneven doping and drain-source electrical field lead to

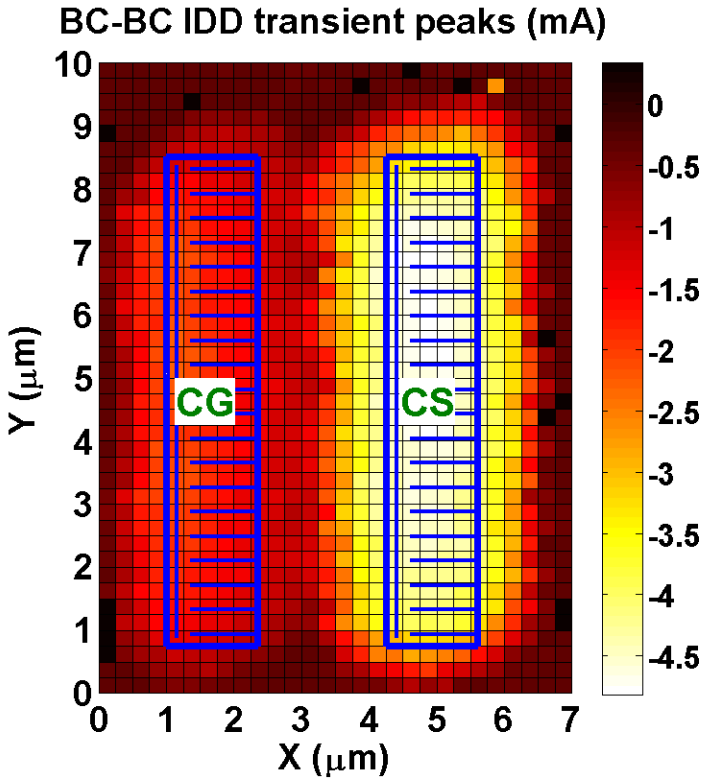


Figure 60: A 2-D raster scan of the top drain (IDD) current transient peaks at locations throughout the sensitive area of the BC-BC cascode structure. The approximate location of the active area of the transistors is denoted by the blue rectangles. As with all the cascodes, strikes of the CS device resulted in higher transient peaks than strikes of the CG device.

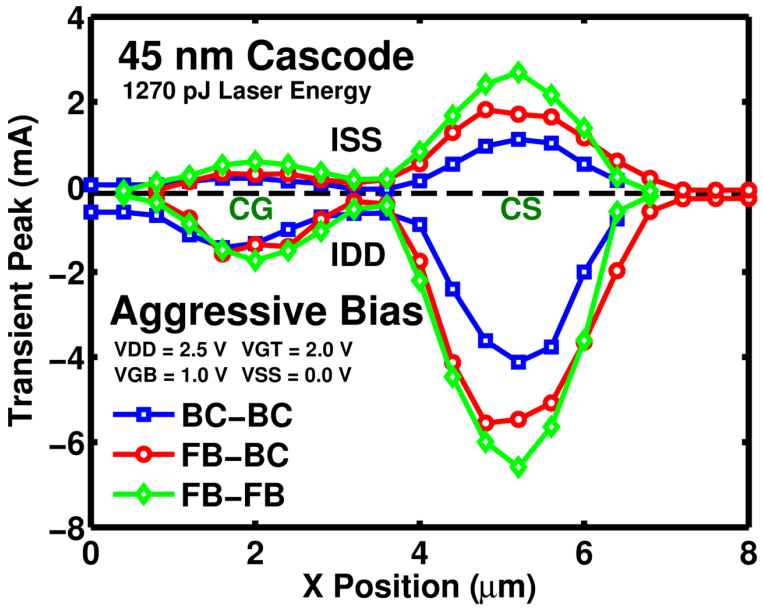


Figure 61: Transient peaks of the bottom source (ISS) and top drain over the width of the two devices in the cascode while in an aggressive bias condition, showing the difference between the responses of the three different configurations. The structures with floating body devices consistently had larger transients.

current flow similar to a bipolar transistor and an overall amplification of collected charge.

The effect was more apparent in the CS device strikes because bipolar amplification was unhindered by CS device loads. During CS strikes, the buffering CG device provided a low-impedance path for electrons to leave the CS device, and the VSS bias-tee presented 50 Ω at high frequencies through the oscilloscope, allowing both holes to leave and electrons to enter the device source in the absence of a body contact. On the other hand, the loading of the CG device inhibited bipolar amplification. During CG strikes, the high-impedance CS drain limited the path for holes to leave and electrons to enter the CG transistor source. As a result, the CG source terminal potential followed the CG body potential rather than conducting as much diffusion current as seen in the CS strike.

Next, the more aggressive bias led to higher magnitude transient peaks from strikes in both devices as seen in Figure 62. The higher drain to source voltages in the aggressive

bias created higher intensity electric fields and enhanced electron-hole separation. Unexpectedly, under the light bias condition only, the two cascodes with a floating-body CS device exhibited a long-lasting transient component during CS strikes, as shown in Figure 63. The longest transients were on the order of 10 μs long and are shown in the inset of Figure 63. Because the transients required the use of a coarser oscilloscope sampling rate (25 MS/s) to capture their entire duration, the peak amplitudes were not consistent with the high sampling rate captures in the main graph of Figure 63.

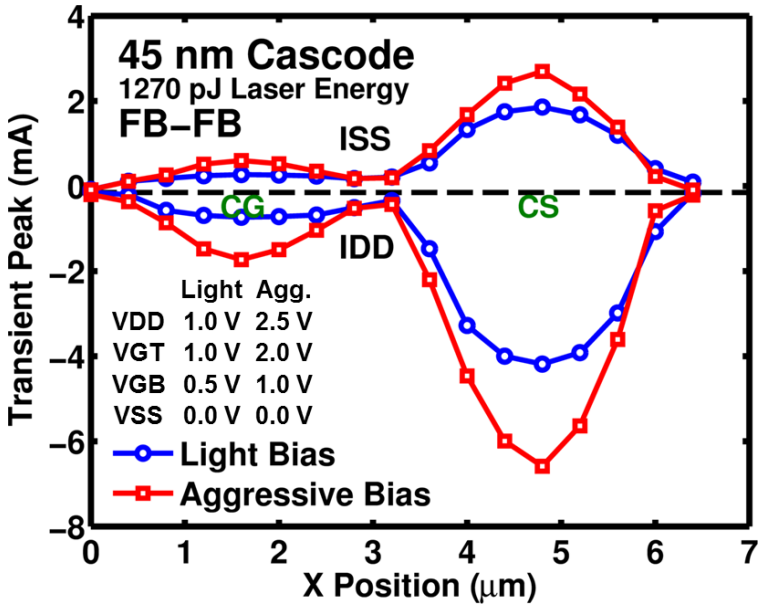


Figure 62: Transient peaks over the width of the two devices in the floating body only cascode, showing the difference between the responses in the two different bias conditions. The more aggressive biasing with higher drain to source voltages resulted in larger peak transients in all three cascode configurations.

4.2.2 TCAD Simulations

Calibrated 2-D TCAD models were developed for the 45 nm cascode cores prior to this work [14] and served to verify trends observed in experiment. Direct transient comparison is not intended. As before, the simulations were carried out using the

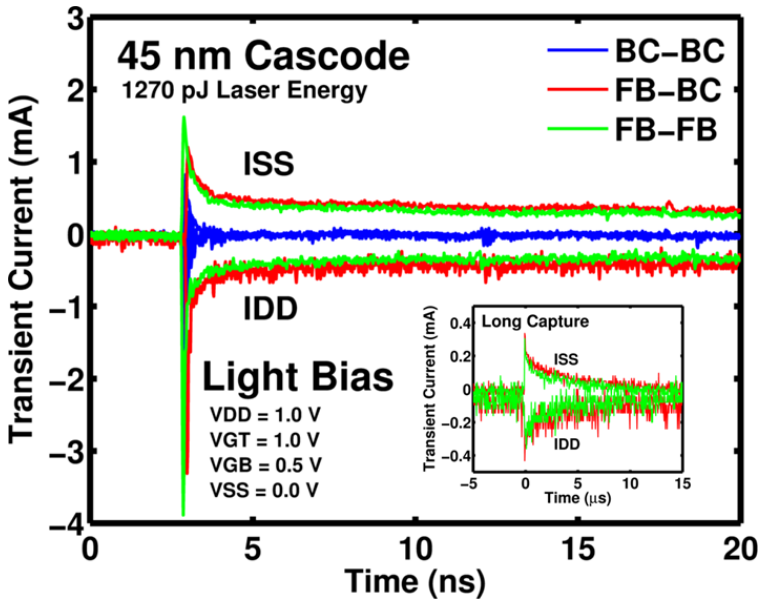


Figure 63: Transient current captures of the resulting transient from charge deposition into the CS device of the cascodes while in the light bias condition, showing the resulting long transient with a floating-body CS device. The inset is a longer but lower sampling rate transient capture showing that the transients are on the order of 10 μs long. The long section disappears in the more aggressive bias condition but, notably, does not occur in the body-contacted CS device in either bias.

Synopsys Sentaurus tools [70]. The simulations were performed with doping concentration and electric field dependent mobility, band-gap narrowing, and University of Bologna impact ionization models [71]. Hydrodynamic transport models were utilized with default parameter values. The two devices in the cascode test structures were simultaneously simulated to better understand the transient mechanisms and because the simulation required the two devices to be self-consistently solved. The source of the CG device and the drain of the CS device were electrically connected using mixed-mode netlisting.

Body-contacting was accomplished with the approximation of setting the potential across the lowest point in the active area, just above the buried oxide, to 0 V as shown by the horizontal line between the bottoms of the two devices in Figure 64. The body contacts in the actual devices were located only on the lower X side in Figure 60 and Figure 61. As the peak transient values across the devices were close

to symmetric about each device x-axis mid-point, it is justifiable in this case that the mere presence of the body-contacts was more important than their specific location for modeling purposes.

The ion strikes were modeled as constant charge deposition paths of 0.4 pC/μm following Gaussian distributions perpendicular to the strike path, simulating an LET of approximately 39 MeV·cm^2/mg. The characteristic radius was chosen to be 0.1 μm. The temporal charge deposition followed a Gaussian function with a characteristic radius of 2 ps centered at 0 s. The ion tracks were centered in the middle of the transistor drains as illustrated by the arrows in Figure 64 where the blue arrow points to the CG device and the red arrow points to the CS device.

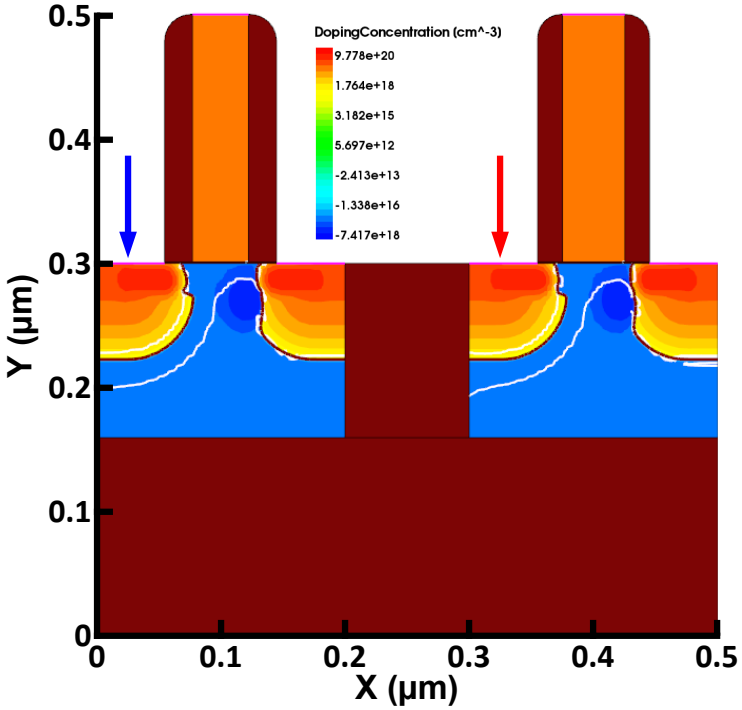


Figure 64: The doping profile of the TCAD model used in the strike simulations to confirm the experimentally observed trends. Body-contacting was accomplished by setting the potential across the lowest point in the active area, just above the buried oxide, to 0 V. The arrows denote the two strike locations used in simulations. The blue arrow points to the CG device, and the red arrow points to the CS device.

Contrasting the TCAD simulations of ion strikes at the two different device drains provided deeper understanding of the observed transients. Horizontal cuts of the

potential in the FB-FB cascode TCAD model in the light bias at the peak of the current transient are shown in Figure 65. In the no strike case, approximately half of the total potential across the cascode is dropped across each device. This places the voltage of the source of the CG device and the drain of the CS device (the internal node) at about half-way between VSS and VDD. The shallow-trench isolation (STI) potential benignly follows the surrounding active areas fringing fields between the source or drain and body. During the strikes, the generated carriers are separated by the electric fields present within each device. While carriers are taken in by the DC voltage source on one terminal of the device, they build up in the internal node, affecting the voltage. The result is that the drain-source voltage across the transistor struck approaches zero.

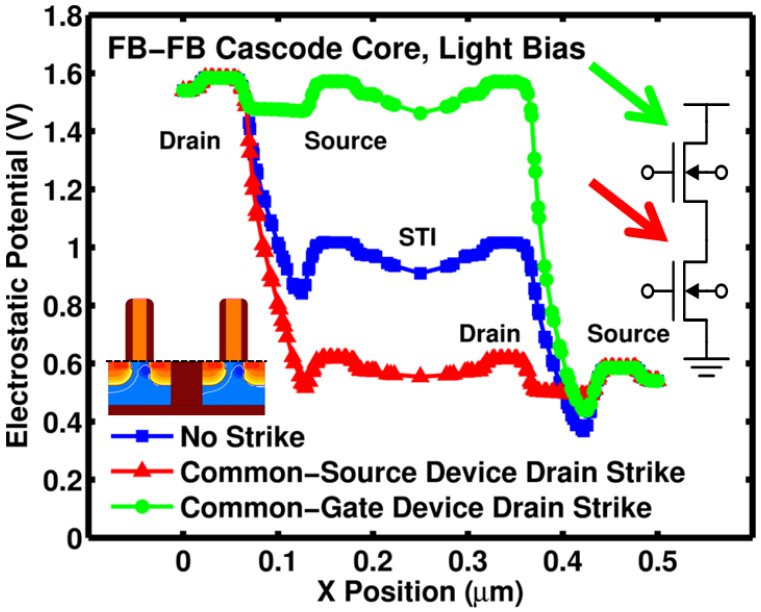


Figure 65: Single-dimension potential cuts in TCAD simulations of the FB-FB cascode taken at the peak of each transient, shown against the no strike case. Comparisons between the two strike locations and the no strike case are shown. The voltage approached zero across the device struck as carriers built up between the two devices.

The carrier transport is symbolically illustrated in Figure 66. In the case of the CS strike, the electric field drives the holes to the CS source terminal and out the

VSS voltage source. At the same time, the electrons are driven to and accumulate in the internal node causing the voltage to fall. The voltage change raises the CG gate to source voltage, which allows the electrons to flow through it to the VDD voltage source via normal FET channel creation. From a small-signal perspective, the carriers leaving the CS device encounter a low-impedance terminal, the source of the CG device, which requires relatively little voltage variation to conduct the carriers through.

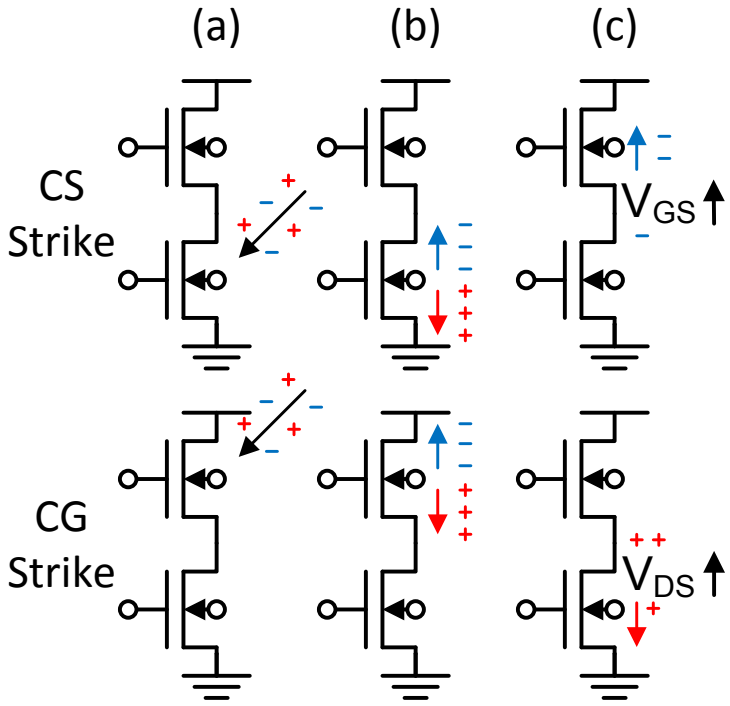


Figure 66: Illustration of the electron and hole transport immediately after the heavy-ion strike in each of the two cascode transistors. (a) represents the initial strike; (b) is the electric field driven carrier separation in the device struck, and (c) is the resulting carrier transport in the un-struck device. The CG device allowed more carrier flow during a CS strike than the CS device during a CG strike.

In the case of the CG strike, the electric field drives the electrons to the CG drain and out the VDD voltage source. At the same time, the holes are driven to the internal node causing the voltage to rise. This potential change raises the CS drain-source voltage, which causes relatively limited current flow via channel-length modulation and drain-induced barrier lowering. Connecting back to the small-signal

explanation, the carriers encounter a high-impedance terminal, the drain of the CS device, which requires relatively large voltage variation to conduct additional current. The simulated IDD transient is plotted in Figure 67 and agreed with the experimental trend: CS strikes resulted in higher magnitude transient currents.

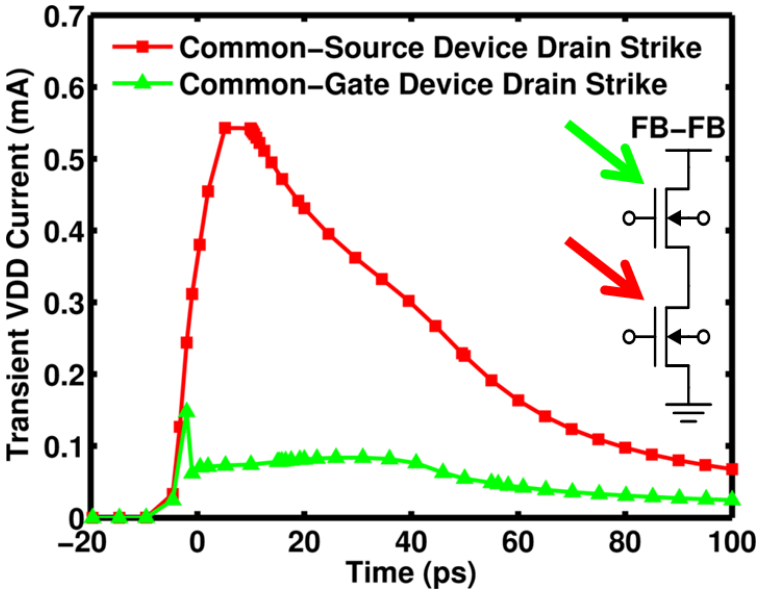


Figure 67: TCAD simulation of transient current variations from DC, showing the amplitude difference when a strike occurs in either the CS or CG device. CS strikes pulled down the internal node, allowing the strike-generated carriers to flow out. CG strikes pulled up the internal node, resulting in comparably less current flow.

In further agreement with measured trends, TCAD simulations showed that the transients from the completely body-contacted cascode core were lower in magnitude than the completely floating-body core. Figure 68 shows the potential variation from DC in the TCAD simulations of the FB-FB and BC-BC cascodes taken at the peak of CS device strike transients in the light bias condition. Both the change in the internal node potential and body-source junction barrier in the CS device were twice as large in the FB-FB cascode compared to the BC-BC. The lowering of the body-source junction barrier in the struck device is indicative of bipolar charge amplification. The resulting transients in the light and aggressive bias schemes are shown in Figure 69. In both biases, the BC-BC transient peaks were slightly lower, and their duration

was less than half of the FB-FB transients. While the differences in peak values were more pronounced in measurement, the discrepancy could be due to the high-frequency content in the transients, which is well above the 12.5 GHz bandwidth of the oscilloscope.

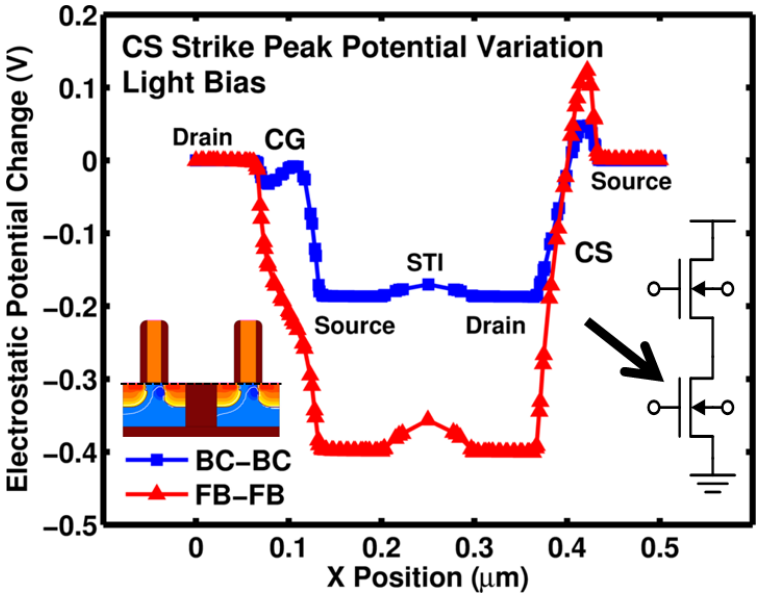


Figure 68: Potential variation from DC in TCAD simulations of the FB-FB and BC-BC cascodes taken at the peak of CS device strike transients in the light bias condition. The variation of the internal node and CS body-source junction barrier in the FB-FB cascode was twice that of the BC-BC.

The effect of bias on the transient signature of the floating-body cascode cores was also confirmed in TCAD simulation. As shown in Figure 70, the transient resulting from a strike within the CS device of the FB-FB cascode core had a higher peak but shorter duration as compared to the same strike in the lighter bias scheme. In both simulation and measurement, the amount of collected charge was less in the aggressive bias despite the higher peak current. The difference between the bias states in simulation could be attributed to the larger DC current and better high-frequency performance [14] in the aggressive bias allowing the cascode to discharge more quickly. However, the contrast in measurement was much larger, leading to the conclusion that the either the effect is exacerbated by the testing conditions, possibly

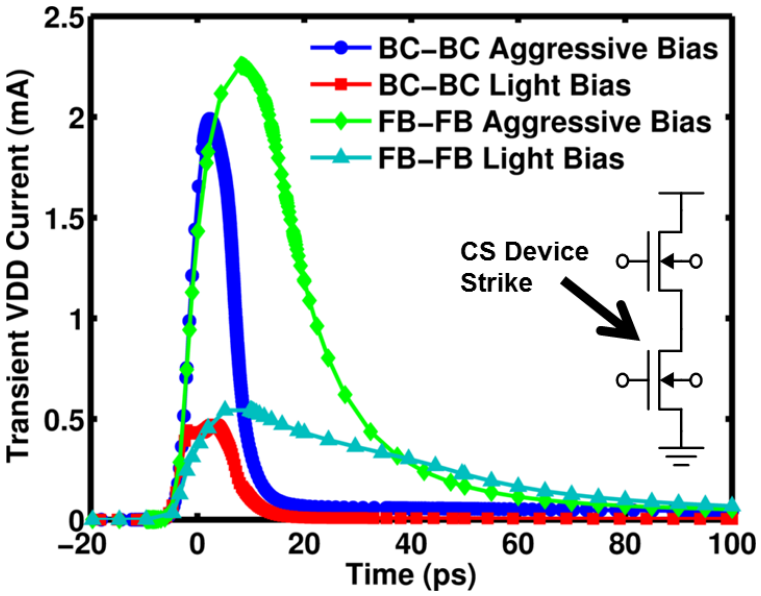


Figure 69: TCAD simulation of transient current variations from DC with the common-source device being struck, illustrating how body contacting reduces the peak and duration of the resulting transient in both the light and aggressive bias conditions.

the impedance of the bias-tees, or is not covered in the TCAD model. In either case, more investigation is needed of the transient elongation at light bias.

4.2.3 32 nm Differential Pair

During the 32 nm differential pair experiment, two challenges were encountered. First, an appreciable amount of current was measured traveling into the V_{IN1} terminal. Unfortunately, this current created an offset in the bias of the differential pair, and severity of the offset varied based on the input bias. It was observed to have a strong dependence on V_{GD1}, so it was characterized as gate-drain leakage. As a result, a distinction will always be made between bias sweeps that vary differential input voltage and those that vary the differential current in the pair. Second, the transients were slightly obscured by a periodic interference signal that was independent of the strikes themselves. To correct for this error, the interference has been mathematically subtracted out from the transients presented using the signals captured during strikes outside the sensitive areas of the transistors (ones that did not cause transients). To

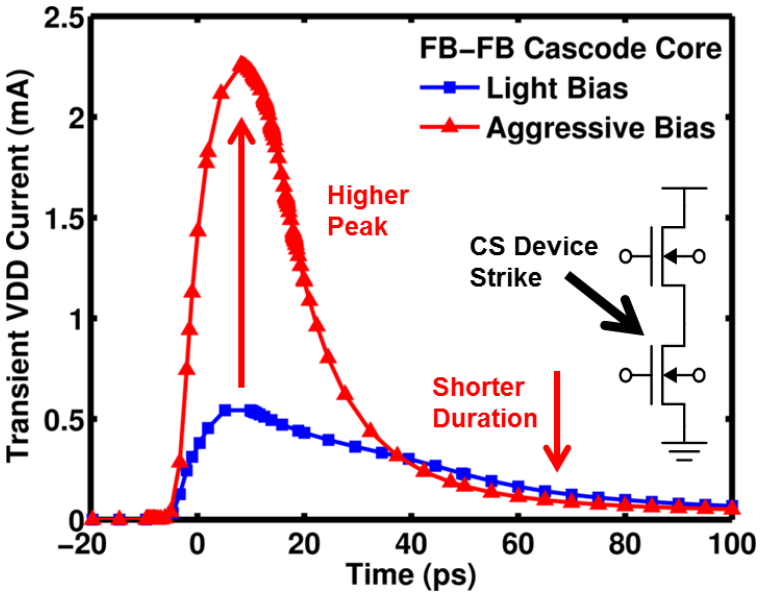
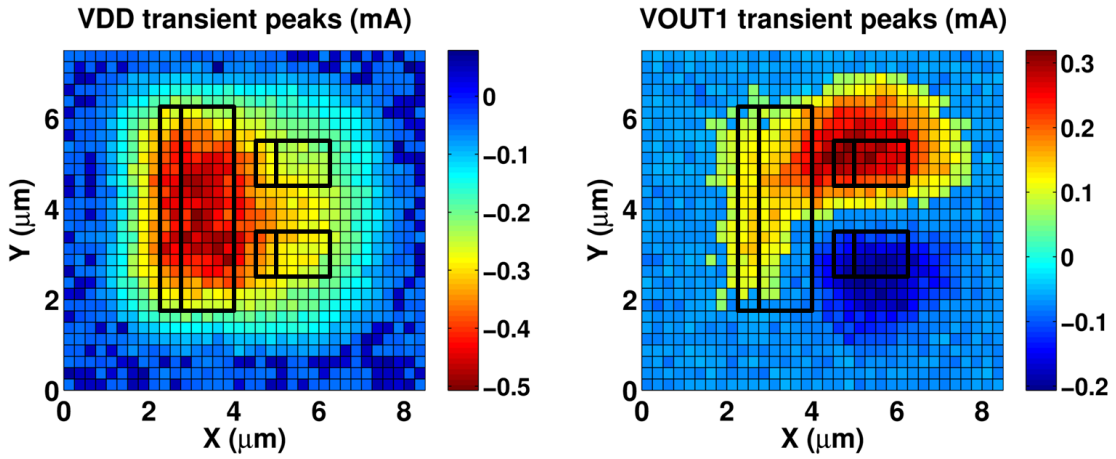


Figure 70: TCAD simulation of transient current variations from DC with the common-source device in the cascode core being struck, illustrating how the more aggressive biasing results in higher peaks but faster recovery in the floating-body cascode core variants. The integrated collected charge was actually less for the aggressive bias.

complete the correction, charge collection graphs are presented with data relative to the no strike case.

The differential pair structure was first analyzed for areas of SET sensitivity. 2-D raster scans (Figure 71) showed immediately that each of the three transistors had a distinct transient signature when struck. Charge deposition into the tail transistor resulted in transients at all three terminals. The V_{DD} terminal exhibited a negative transient, but the two output terminals had positive transients as shown in Figure 72. The negative transient was comprised of the electrons leaving the device and coupling into the oscilloscope. At the same time, the excess holes split between the two differential pair transistors, resulting in transients at both outputs.

Interestingly, the weighing of the split was directly related to the differential bias of the pair. The device with the greater share of the tail current also collected a greater amount of charge as shown in Figure 73. Negative differential current favors M_1, so on the negative bias side, the collected charge is larger from V_{OUT1} while the



(a) (b)

Figure 71: 2-D raster scans of the V_{DD} (a) and V_{OUT1} (b) current transient peaks at locations throughout the sensitive area of the differential pair structure. The estimated location of the transistors is denoted by the pairs of black rectangles where the largest of each pair is the active area and the smaller is the body-contact area.

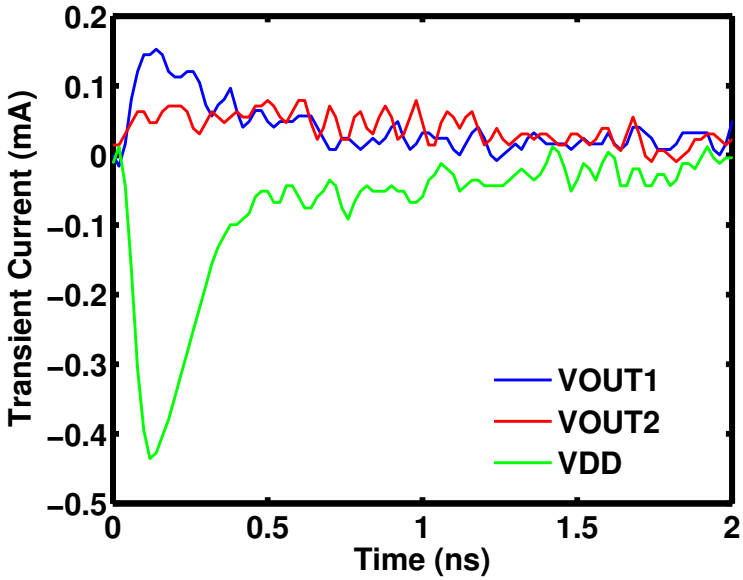


Figure 72: Resulting transients from charge deposition in M_{TAIL}. The interfering signal has been removed based on strikes outside the sensitive area. M_{TAIL} strikes tended to result in a negative V_{DD} transient and positive transients from both V_{OUT} terminals.

collected charge from V_{OUT2} is below the noise floor. The same is true for M_2 with some offset on the positive bias side of Figure 73. It is worth noting that the collected charge from each output is equal near balanced current bias, making the differential integrated charge zero. In a differential output topology like this one, equal signals on both outputs would likely be rejected by the input of the next circuit block, so strikes on the tail transistor with a balanced differential bias will be unlikely to cause disruptions in the signal path.

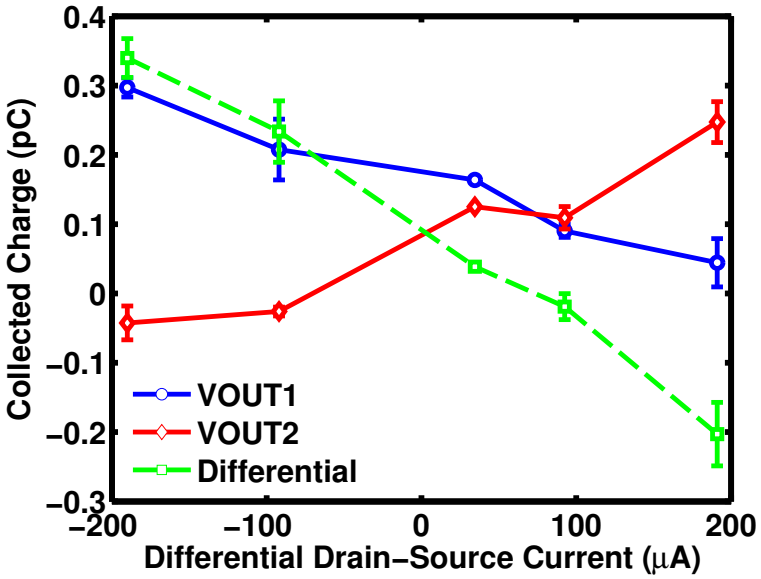


Figure 73: Collected charge from the two differential outputs from strikes in the center of M_{TAIL}. As the tail current is switched from one side of the differential pair to the other, the transient collected charge follows.

The last two transient signatures were observed from charge deposition into the differential pair transistors. Both signatures followed a similar pattern. Charge deposition into a differential pair transistor resulted in three transients: a positive transient at the adjacent output, a negative transient at the opposite output with a smaller peak and nearly equal but opposite collected charge, and a negative transient at V_{DD} with an appreciable peak but little collected charge as illustrated by the transients resulting from an M_2 strike shown in Figure 74.

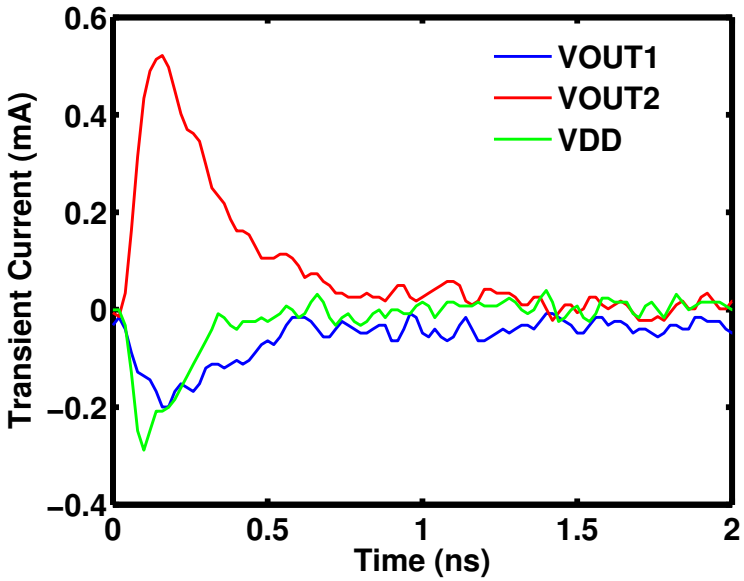


Figure 74: Resulting transients from charge deposition in M_2. The interfering signal has been removed based on strikes outside the sensitive area. Differential pair strikes tend to result in a positive transient on the adjacent output and negative transients at V_{DD} and the opposite output.

During a differential pair strike, electrons and holes were first separated by the device's electric fields, then they began to discharge throughout the structure. The transient at the adjacent output was made up of the holes leaving the device and coupling into the oscilloscope. The electrons had two discharge paths: the tail transistor and the opposite pair transistor. The opposite pair transistor allowed more charge conduction through normal FET channel creation as the electron buildup caused the voltage at the shared node to fall. The short peak at V_{DD} could have originated from the charging of the reverse-biased drain-body diode or channel-length modulation as the $V_{DS.TAIL}$ magnitude increased.

The effect of the common-mode input bias on the differential pair transient peaks is shown in Figure 75, where the dashed lines represent the measurement noise floor. When the common-mode input bias was increased from 0.1 V to 0.5 V, almost all transient peak magnitudes increased. The higher common-mode bias increased the

magnitude of the drain-source voltage across the transistors, which has been known to increase transient peaks.

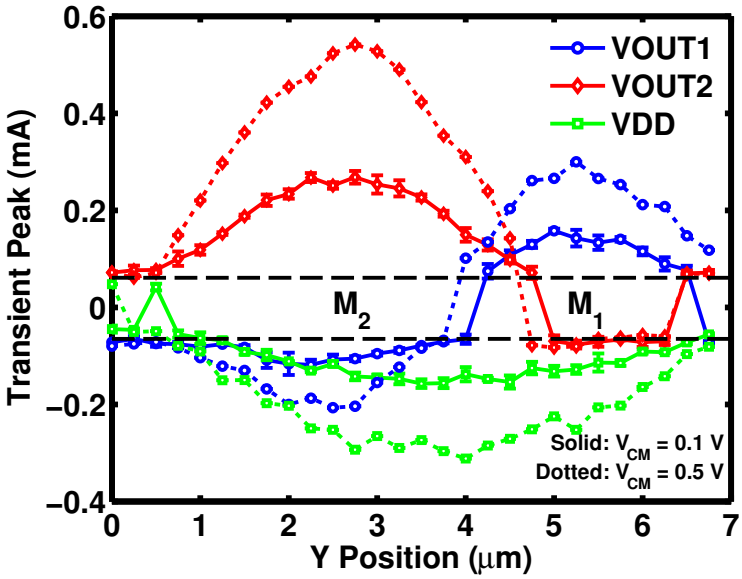


Figure 75: 1-D cut across the differential pair transistors showing the resulting transient peaks. The black lines represent the noise floor. The higher common-mode voltage results in larger magnitude transient peaks.

The effect of the common-mode input bias on the transient collected charge is shown in Figure 76. For both biases and strike locations, the general pattern was consistent; the outputs had nearly equal and opposite collected charge, and the V_{DD} terminal had significantly less than V_{OUT1} and V_{OUT2}. At the higher common-mode bias, the collected charge increased slightly at the output terminals for strikes in M_2 but increased by as much as 50 % for strikes in M_1.

The differential input bias also had an effect on transients from strikes of the differential pair devices. As the current was shifted to one branch, collected charge fell faster in the device with more current. As a result, the collected charge at negative differential current (more in M_1) was larger for strikes in M_2, and the collected charge at positive differential current was larger for strikes in M_1 as shown in Figure 77. The

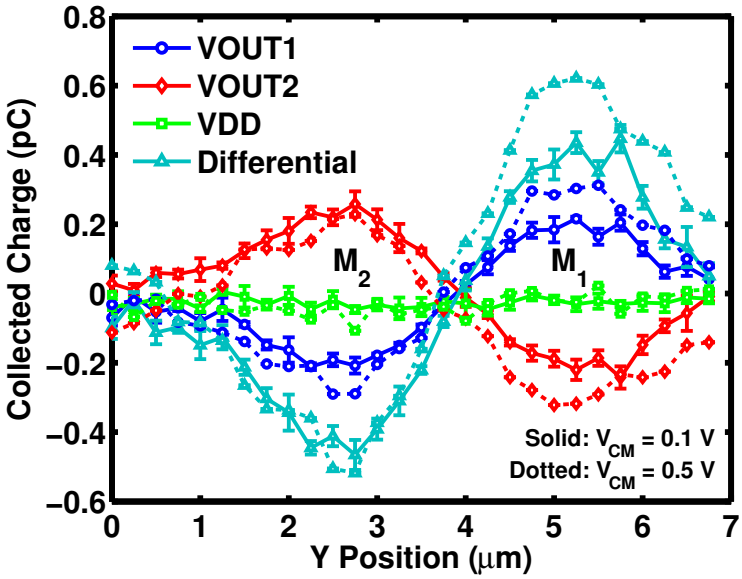


Figure 76: 1-D cut across the differential pair transistors showing the resulting collected charge. The higher common-mode voltage results in a slight increase of the collected charge at the output terminals from strikes in M_1 but not in M_2.

difference can be explained by the smaller magnitude drain-source voltage across the device with more absolute current. Again, less potential drop across the device lowers the transient.

Strangely, the maximum transients occurred near balanced bias. Because the magnitude of the V_{DS} was decreasing, it was expected and observed that the device receiving more current in the differential pair would generate lower magnitude transients. It was not expected that the device with less current (larger V_{DS}) would also see a reduction in transients. This could be explained by the results of the single-device exposures in the next section. The 32 nm devices exhibited an increasing collected charge versus V_{DS} up to the rated voltage of 0.9 V. Above 0.9 V, the collected charge decreased. The same mechanisms could have been responsible for the reduction in collected charge in off-side of the differential pair as the voltages increased beyond 0.9 V. An in-depth review of these mechanisms is a candidate topic of future work.

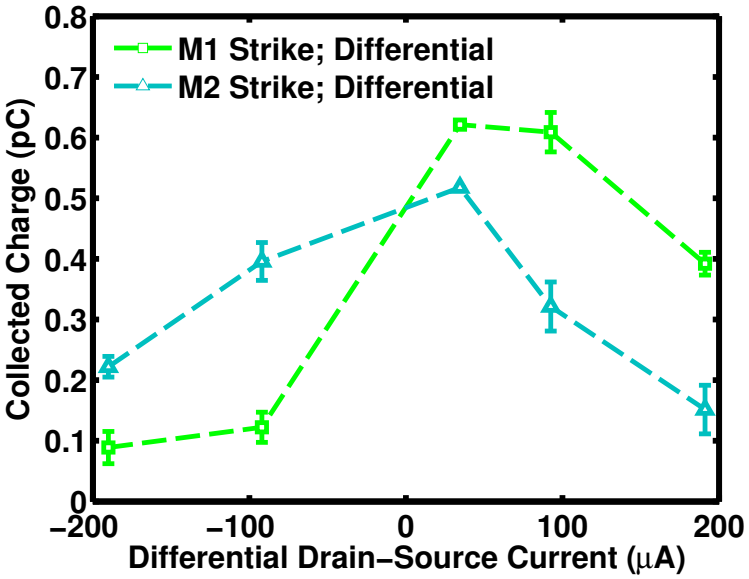


Figure 77: Absolute value of differential collected charge from the outputs of the differential pair from charge deposition in each differential pair transistor. The magnitude of collected charge tends to be larger for transistor with less current.

4.2.4 Single-device Exposures

Stand-alone 45 nm multi-finger devices were tested for comparisons of body-contacting. The results were consistent with the cascodes and indicated the presence of bipolar amplification in the floating-body (FB) device. The FB MOSFET had consistently greater magnitude peaks and collected charge over all laser energies (Figure 78). Even at higher laser energies, when the transient peaks saturated near the same value, the collected charge from the floating-body device was almost double that of the similar body-contacted device despite having less than half the drain area, noted back in Table 6.

The last experimental comparison was the effect of technology scaling on SETs (45 nm vs. 32 nm). The devices tested had drawn sizes and threshold voltages as noted in Table 7 and were all floating-body transistors. Each was positioned at the point of largest peak transient during exposure. It was experimentally shown that the 32 nm regular threshold voltage devices charge collection was the highest of the devices above

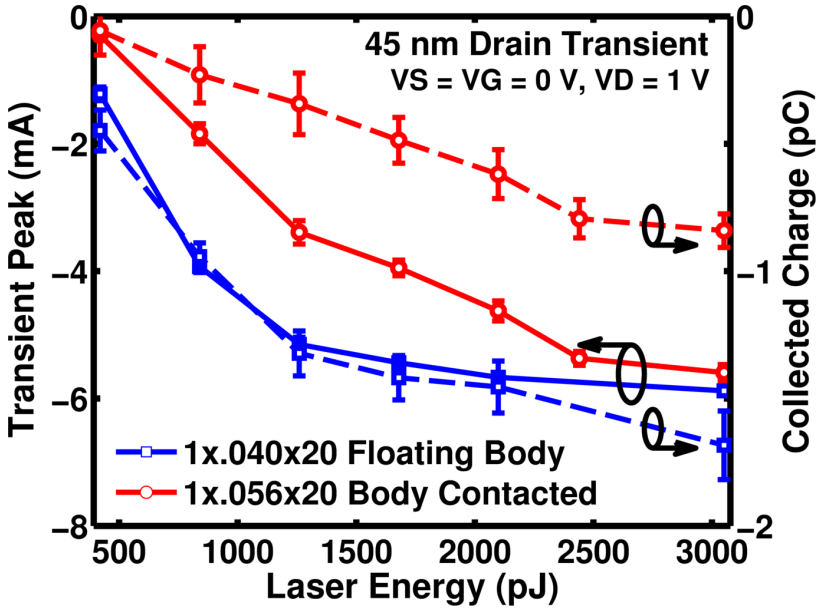


Figure 78: Transient peaks and charge collection versus laser energy for the 45 nm multi-finger devices of the same geometry as those in the cascode structures. The floating body device had consistently greater magnitude peaks and approximately double the collected charge even with half the drain area.

V_{DS} of 0.5 V (Figure 79). At voltages close to and above the recommended voltage rating for this technology, V_{DS} = 0.9 V, the charge collection decreases but is still greater than the others. Furthermore, the 32 nm analog threshold voltage device had higher collected charge than the 45 nm analog threshold voltage device over most drain-source voltages despite the lower drawn width. If the charge collection were normalized to drawn width, the two 32 nm devices would line up similarly between V_{DS} values of 0.5 V and 0.9 V, but both would have larger charge collection than the 45 nm device above V_{DS} values of 0.5 V.

Table 7: Single-finger Devices Tested

Process	Width (μm)	Length (μm)	Threshold
32 nm	2.08	.040	Regular
32 nm	1.00	.048	Analog
45 nm	2.00	.040	Analog

When tested over laser energy, the 32 nm regular threshold device consistently exhibited higher collected charge than the other devices, as seen in Figure 80. At the

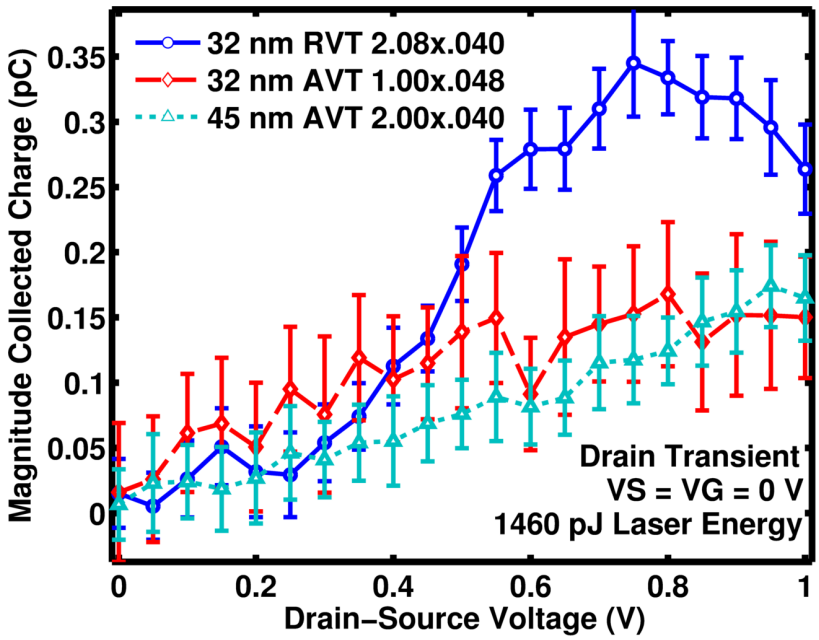


Figure 79: Transient collected charge magnitude versus drain voltage for the single-finger devices. The regular threshold 32 nm device was consistently the worst-performing of the three tested, and the analog threshold 45 nm device was most often the best across the voltages. If normalized by drawn width, the collected charge in the 32 nm devices would be similar for $V_{DS} > 0.5$ V, and both would be approximately double the 45-nm device.

lower experimental energies, the 45 nm analog threshold device had the lowest collected charge of the three. If normalized to drawn width, the 32 nm analog threshold device would have the highest collected charge across all energies, while the 45 nm device would have the lowest. In both measurements, the 45 nm analog threshold device consistently had lower collected charge in both raw and normalized comparisons to the two 32 nm devices.

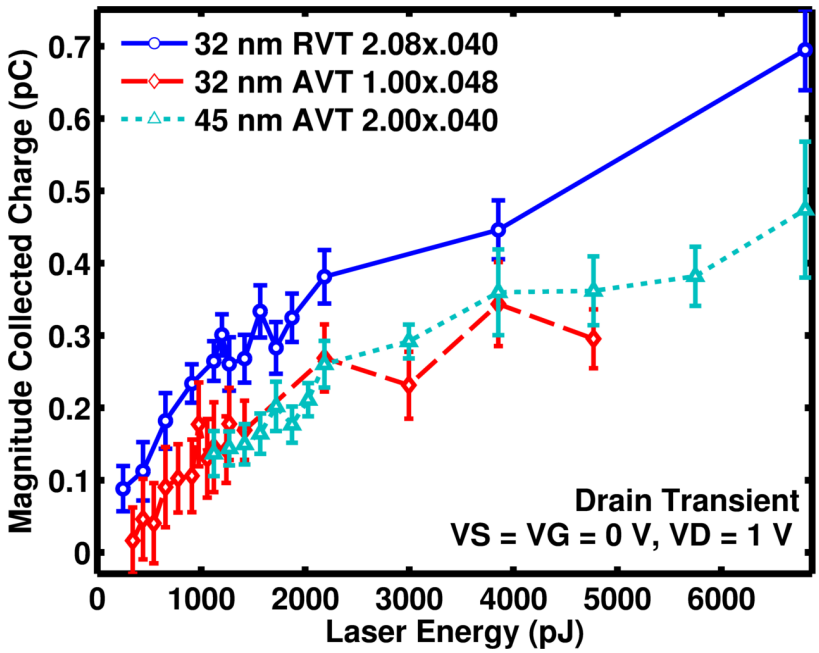


Figure 80: Transient collected charge magnitude versus laser energy for the single-finger devices. The 32 nm regular threshold voltage device consistently exhibited higher collected charge over the experimental energy levels. If normalized by drawn width, the 32-nm analog threshold device would have the largest collected charge of the three, and the 45-nm device would have the least.

4.3 Summary and Implications

This work used charge deposition by TPA and calibrated TCAD simulations to provide a thorough study of the single event transient response of the cascode structure in a modern 45 nm RF-CMOS/SOI technology and the differential pair circuit block in a cutting-edge 32 nm RF-CMOS/SOI technology. It was found that the transients propagate much like analog/RF signals, following basic small-signal rules in both the

cascode cores and differential pair structures.

In addition, given the proven efficacy of body contacting schemes in reducing transients, body-contacted cascodes will provide noticeably better hardness against SETs than floating-body cascodes. In performance constrained designs that require floating-body devices, biasing them more aggressively has been shown to shorten the duration and collected charge of SETs in both measurement and simulation. Looking toward the future, designs in 32 nm may be more susceptible to SETs than similar ones in 45 nm due to the increased collected charge, even with reductions in sensitive area.

CHAPTER V

CONCLUSION

This work gained new understanding of the best practices in analog circuit design for both wide temperature ranges and radiation exposure. The analog/mixed-signal system, the SiGe Remote Electronics Unit, and the two transceivers designed for the RS-485 and ISO 11898 were all validated over a wide-temperature range, and both the SiGe REU and the ISO 11898 transceiver were shown to be tolerant to total ionizing dose radiation exposure. Study of both the transceivers and the REU resulted in further understanding of single-event effects. A SiGe BiCMOS technology with a second-generation SiGe HBT and 0.18 μm CMOS was used to design low-noise voltage references for a cryogenic environment. The references used low-noise SiGe HBTs alongside negative feedback techniques to mitigate the largest noise contributors at both 300 K and 90 K. Lastly, the radiation tolerance of deep sub-micron CMOS in silicon-on-insulator (SOI) processes was studied, resulting in new knowledge of the behavior of single-event transients in analog and RF circuits and further evidence of scaling trends of single-event effects in these processes. Transients were found to follow the same small-signal rules used in analog circuit design.

5.1 Future Work

Significant opportunities exist for future work stemming from this research.

- The SiGe Remote Electronics Unit represents the cutting-edge in extreme-environment electronics and could be leveraged in future NASA designs, such as the Orion Multi-Purpose Crew Vehicle, the Space Launch System, or the next Martian rover.

- The liquid-argon time-projection chamber proposed for the US Long Baseline Neutrino Experiment Study will require more extensive electronics and makes for a perfect fit for the advanced analog performance of SiGe BiCMOS technologies. Designs like linear voltage regulators and laser drivers would be ideal for the future of the experiment.

- The availability of a calibrated TCAD model of the 45 nm SOI CMOS platform studied in this research was instrumental in the analysis of the single-event transient response. A similar opportunity exists in the latest 32 nm technology from IBM. Calibration of a 2-D nMOS TCAD model would begin to enable basic SEE simulation. It could be used to explain the interesting peaking of collected charge near the rated voltage of the process. A more complex pFET model taking into account the SiGe source and drain areas, would be a very compelling body of work.

- This research presented basic circuit structures, the cascode and differential pair, and found that small-signal analysis could predict the first-order single-event transient responses. Analysis of more complex blocks could begin to truly connect the single-device to circuit response to SETs.

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